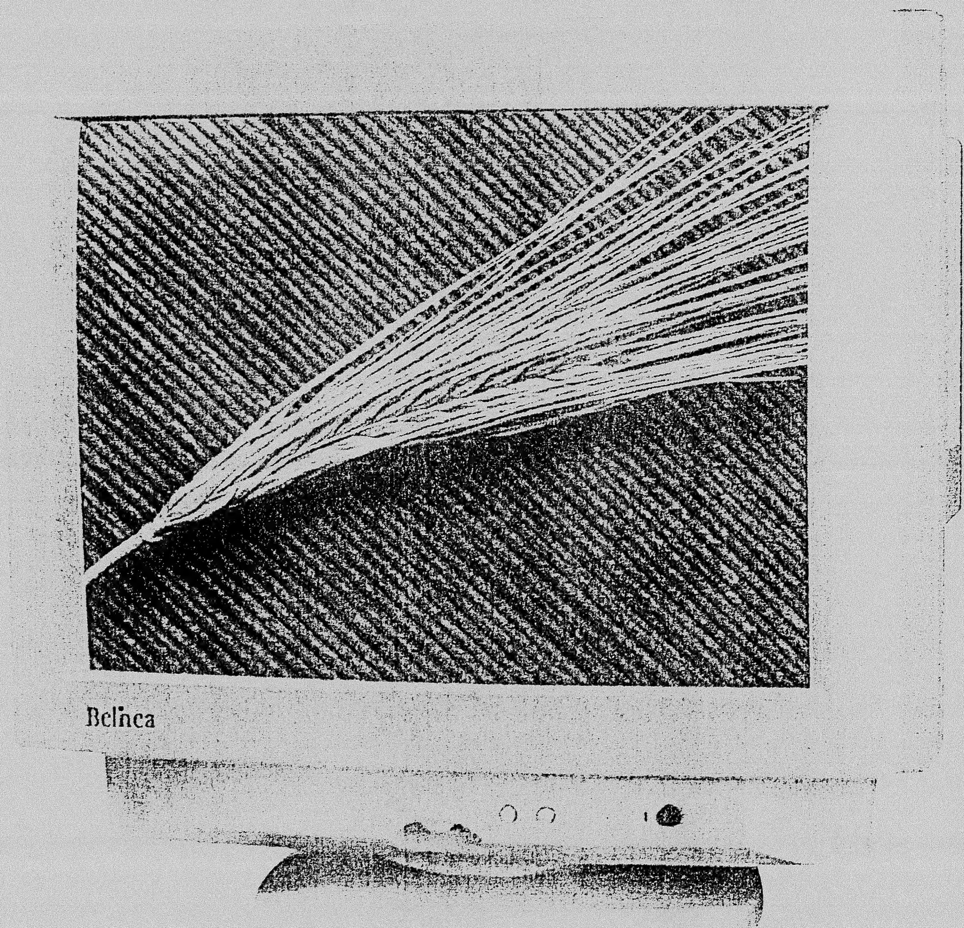
Belinea 10 80 50

Color Monitor
Service Manual



Preface
Before You Start

General Safety Precautions

1. Use an isolation transformer in the power line and AC supply to troubleshoot.
2. When servicing, observe the original lead dress, especially in the high voltage circuits. If a short circuit is found, replace all parts which have been overheated or damaged.
3. Potentials, as high as 25kV are present when this display is in operation. Operation of the display without the rear cover involves the danger of a shock hazard from the display power supply. Servicing should not be attempted by anyone who is not thoroughly familiar with the precautions necessary when working on high voltage equipment. Always discharge the anode of the picture tube to the display chassis before handling the tube.
4. After servicing, be sure to check the items listed in the Safety Checkout, below before returning the serviced unit to the customer.

Safety Checkout

The following checks must be made after correcting the original service problem and before the unit is returned to the customer.

1. Check the area of your repair for unsoldered or poorly soldered connections. Check the entire board surface for solder splashes and bridges.
2. Check the inter board wiring to ensure that no wires are pinched or coated with high-wattage resistors.
3. Check that all control knobs, shields, covers, ground straps and mounting hardware have been replaced. Makde absolutely sure you have replaced all the insulators.
4. Look for any unauthorized replacement parts, particularly transistors, that may have been installed dueing a previous repair. Point them out to the cusstomer land recommend their replacement.
5. Look for parts which, though functioning, show obvious signs of deterioration. Point them out to the customer and recommend their replacement.
6. Check the line cord for cracks and abrasion. Recommend the replacement of any such line cord to the customer.
7. After making any repair, check the B+ and HV to see whether they are at the values specified. Make sure your instruments are accurate; if your HV meter always shows a low HV, check the meter to ensure it is not malfunctioning.
8. Carry out the leakage current checks as detailed below overleaf.

Leakage Current Cold Check

1. Unplug the AC cord and connect a jumper between the two prongs on the plug.
2. Turn on the display power switch.
3. Use an ohmmeter to measure the resistance value between the jumpered AC plug and each exposed metallic cabint part on the display, such as screwheads, terminals control shafts, etc. When an exposed metallic part has a return path to the chassis. the reading should be between 240k and 5.2M. When exposed metal does not have a return path to the chassis, the reading must be.

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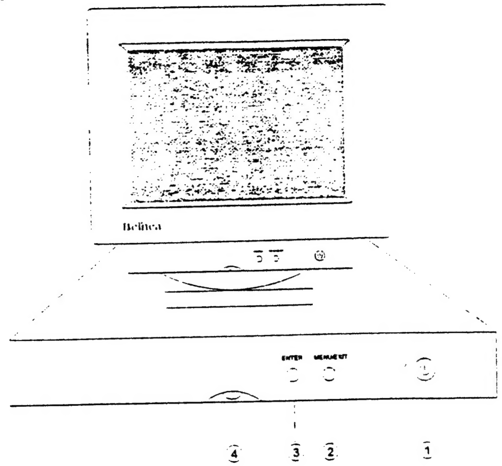
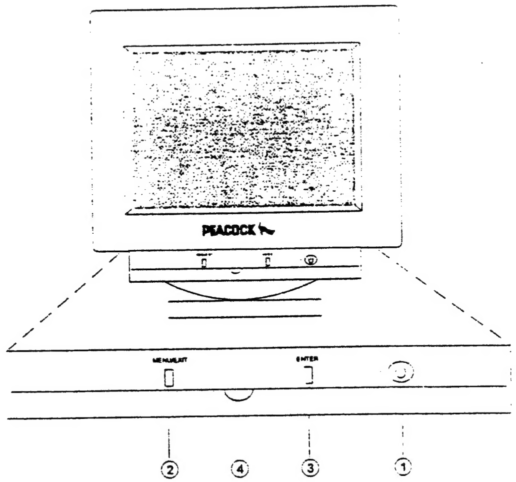
Notes

1.1. Monitor Control Locations & Functions

□ Model NO. : RTH-1H21



□ Model NO. : RTH-1H26



KEY TO BUILT-IN MONITOR CONTROL FUNCTIONS		
①	Power ON/OFF switch	Hard power ON/OFF button. Adjacent LED is lit when on. The LED color is green for normal condition and change to orange for DPMS condition.
②	Menu/Exit button	Press to access into main OSD function, press again to exit OSD function from latter stage into former stage.
③	Enter button	Press to confirm OSD function and value setting.
④	Thumbwheel control	Thumbwheel control is for contrast adjustment at normal operation. For OSD operation, used as function selection and adjustment.

4. Remove the power switch.
5. Remove the four screws from the control board. Refer to the figure 2-8 (B).
6. Remove the control board.

2.7.2. Model NO. : RTH-1H26

1. Remove the three screws from the control board. Refer to the figure 2-8 (B).
2. Remove the control board.

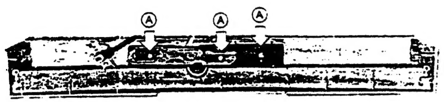


Figure 2-9 Remove the Control Board

Section 3.

Theory of Operation

3.1. Switching Power Supply

The switching power supply (SPS) used in this display is a 150W flyback mode type. The power supply provides six outputs (215V, 78V, 15V, -12V, 6.3V and +5V). Please refer to schematic diagram for details of the circuit layout. The input voltage is from 88VAC — 264VAC with an input frequency of 47Hz — 63Hz. as shown in figure 3-1.

The current first passes through the EMI control circuit and is regulated to DC by the bridge diode (BD901) and filter capacitor (C907). During rectification a large current surge is generated and as C907 has a very low impedance while being charged the fuse, on/off switch and bridge diode are all liable to be damaged. For this reason, a thermal resistor (NTCR) is added before the bridge diode in order to limit the large current surge generated during the charging of the capacitor.

During rectification, C910 is charged through R903 and R904. When C910 is charged to 16V, IC901 3842A starts to operate (for details, of the functions of this IC, please refer to the relevant data sheet) and outputs a pulse signal from Pin 6 to set the transistor Q902 in the ON state. At this time, transformer T903, which is connected in parallel, starts to store power. When the current passing through the resistor R914, and the supplementary current from R957 and R964 into Pin 3 of IC901 reaches 1.1V, IC901 is reset, causing the energy stored by the transformer to reach the rated value. In order to prevent the transformer from being saturated and causing damage to the transistor, when transistor Q902 is in the OFF state, the energy stored in the transformer T903 is released into the secondary coil and is regulated through the various output loops and filters and converted to the required DC output. In addition to this, at the appropriate time, the windings pin1 — pin2 supply Pin 7 of IC901 with a fixed power supply for normal operation. Also, when windings pin2 — pin3 are in power saving active state, power is supplied to Pin 7 of IC901 for normal operation.

In any of the above cased, the output pulse is terminated and the FET is turned off, causing the voltage on the output of the FET to rise rapidly, and the voltage across the winding of the primary to reverse in polarity, thus tending to reset the flux within the core. At this point, the diodes D915, D916, D918-D920, D925 and D926 on the secondary supply winding become forward biased and begin to conduct, thus transferring energy from primary to the secondary, and charging the secondary capacitors.

There is also secondary winding the primary side of the power supply which, through diode D908 and Q901 recharges the control IC901 reservoir capacitor C910. This supply then keep the IC901 running. In the event of a secondary short circuit, the supply fails to recharge, thus the voltage across C910 drops to a threshold limit below which the IC901 cuts out and returns to its low current load operation.

During normal operation, the supply rails charge until the error amplifier realized by IC903 on the secondary begins to turn on the opto-coupler, PH901. At this point, the photo-transistor of this opto-coupler on the primary side begins to conduct, draining current from the primary control IC901 supply through diode D907 and D928.

Under normal operation IC903 regulates the current flow through PH901, and hence determines the output voltage of the error amplifier internal to IC901. Various passive components around IC903 and IC901 set the gain compensation for optimum stability and regulation characteristics.

In the event of a fault condition occurring, either Q904 may be turned on by the lack of voltage at pin2 of IC901 or zener diode ZD903 may conduct, due to excessive voltage on the primary IC901 supply. In the latter case, the triac Q903 will fire, thus dragging down the output of the control IC901 error amplifier, which in turn will limit the duty cycle and reduce the output voltage. It will stay in this mode until the AC input power is removed.

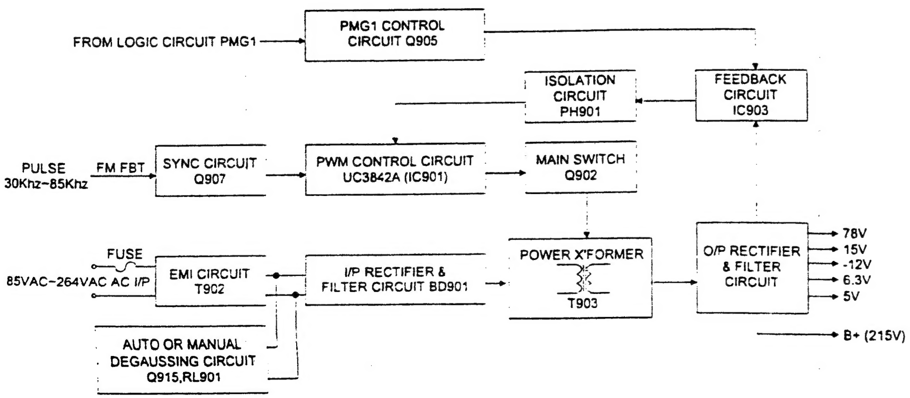


Figure 3-1 Switching Power Supply Block Diagram

When the feedback signal passing through the main 78V output is completed, the transistor's duty cycle is adjusted through the transfer to Pin 2 of IC901 3842A of the primary coil by PH901 4N35 and IC903 TL431, stabilizing the output current. At this time, it is important to note that before the feedback signal is established, the charge level of C917 cannot trigger Q903 SCR or it will cause a faulty power startup. In addition, in order to synchronize the supply power and monitor and reduce noise that will cause interference to the display, in the area D913 the monitor's feedback transformer gets a feedback signal in order to ensure synchronization between the power supply and monitor, with synchronization in the range 30kHz — 85kHz. Because the power operating frequency changes with the monitor causing changes in the value of IP, (the value of LP is fixed while the value of IP increase or decreases according to the frequency), this affects the test value of Pin 3 of IC901 3842A. This causes the total power supplied to vary according to the frequency, so a compensation value is provided by D914 in order to reduce the difference in total power for different frequencies. In addition, because the AC input ranges from 85VAC to 264VAC, this causes the value of the direct current on the DC bus to vary, affecting the rise rate of IP, the oscillator and the duty cycle, and causing the test value obtained at Pin 3 of IC901 to vary. To resolve this, a compensation value is provided by R964 and R957 which reduces the difference resulting from the different input voltages.

3.1.1. Auto-degaussing

When base of Q915 connector is in high state, the transistor Q915 2SC945P is on, causing the relay to jump from Normal Open (N.O.) to Normal Close (N.C.) to perform auto-degaussing operations. The duration of this operation is controlled by a logic pulse and lasts approximately 6 (six) seconds. When transistor Q915 enters the OFF state and the relay returns to N.O. to terminate the auto-degaussing operation is completed.

3.1.2. Suspend Mode Operation

Two feedback ratios can be selected, both sensing from the 78V rail. In the event of Q905 being turned on by micro processor, additional current is drawn from the virtual earth node of IC903, thus causing the power supply to serve the rail to a high voltage, nominally 78V. This is trimmed by resistor R937, R940 and R941. The other supply rail are predetermined ratios of this winging, being +15V, -12V, 6.3V and 215V nominally. In addition, a low voltage primary side winding feeds the control IC901 directly through D907 turning off the control IC901 supply through Q901, which would otherwise dissipate excessively.

When Q905 is turned off, the 78V rail drop to around 17V. In this case, the primary control supply fed through D907 drops to a value that is below the level needed to sustain operation. Instead, Q901 begins to conduct and the higher voltage supply winding taken via D908 is used to keep the primary side powered up with minimal power losses.

The 5V power supply is driven by one of two sources. In normal operation when the 78V is present, the 5V regulator, IC902 is fed from the 15V rail through diode D921. When switched to standby mode (78V rail drops to 12V) then the 15V rail drops too low to supply IC902. In this case Q906 take over and maintains the supply to IC902 at around 9V.

In addition to the 5V regulated supply, in normal operation there is also a 15V regulated supply take from the 15V rail.

To ensure that micro processor gets a good 5V power supply, there is a power good detection circuit formed by Q801 and Q802. This monitors the supply going into the 5V rail (not the 5V rail directly). It detects whether there is sufficient voltage to enable the 5V regulator to work effectively. It is not a detection of the 5V rail itself, but relies upon the premise that the regulator is not faulty and that there is no faulty load condition on the 5V.

During power up, there is a delay to the signal at the output of the threshold comparator Q801 and Q802 a caused by ZD801 and C801, in order to allow the micro circuit time to stabilize. The threshold is chosen such that the RESET line drops low at least 25ms before the 5V drop out of regulation.

Finally a synchronization pulse taken from the horizontal output stage maintains the SMPS operating frequency in sync with the horizontal scan. D913 injects a pulse which prematurely triggers the oscillator within IC901 which would otherwise run at a frequency lower than the minimum required sync frequency.

3.2. The Deflection Circuit

Please refer to the block diagram of the deflection circuit and video circuit and Logic circuit as shown in figure 3-2.

3.2.1. IC301 LM1292 Video PLL System for Continuous-Sync

The LM1292 is an integrated horizontal time base solution specifically designed to operate in continuous-sync video monitors. It automatically synchronizes to any H ferquency from 30kHz to 85kHz and provides the drive pulse to the high power deflection circuit.

Available sync processing includes a vertical sync separator and a composite video sync stripper. An internal sync selection scheme gives highest priority to separate H and V sync, then composite sync, and finally sync on video, no external switching between sync sources is necessary is necessary. The LM1292 provides polarity-normalized H/HV and V sync outputs, along with logic flags which show the respective input polarities.

The design uses an on-chip FVC (Frequency to Voltage Converter) to set the center frequency of the VCO

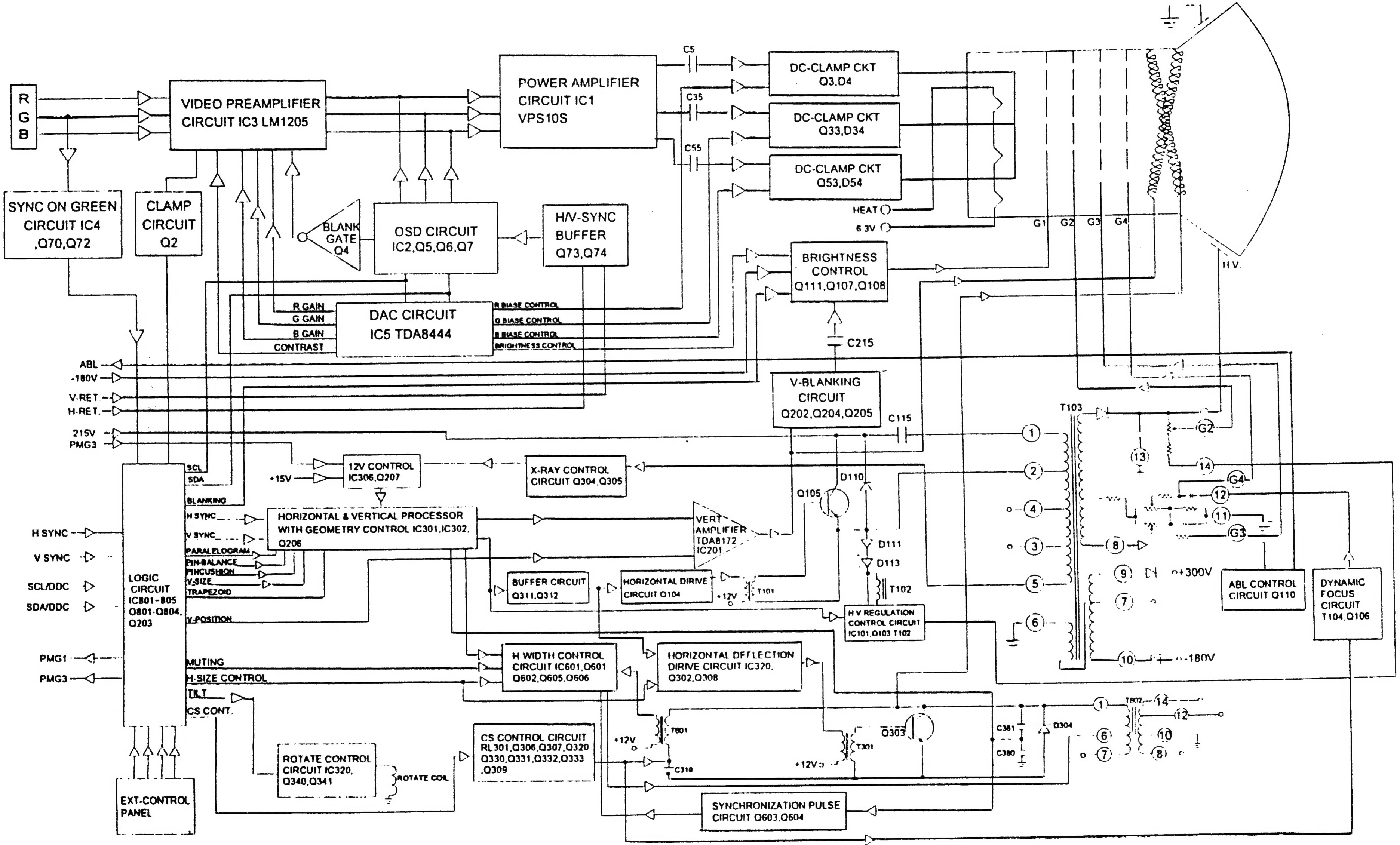


Figure 3-2 Video,Logic,Audio and Deflection Block Diagram

(Voltage Controlled Oscillator). This technique allows autosync operation over the entire frequency range using just one optimized set of external components.

The system includes a second phase detector which compensates for storage time variation in the horizontal output transistor, the picture's horizontal position is thus independent of temperature and component variance.

The LM1292 provides DC control pins for H drive duty cycle and flyback phase.

3.2.2. IC301 LM1292 Pin Descriptions

Pin 1 FVC CAP 2:
Secondary FVC filter pin. Cfvc2 is connected from this pin to ground. The width of the VIDEO MUTE (pin 4) pulse is controlled by the time constant difference between the filters at pins 1 and 25.

Pin 2 Clamp Control:
This low impedance current mode input pin is internally biased to 2V. The direction of current sets the pulse position, while the current magnitude sets the pulse width. A voltage below 2V positions the pulse on the back porch of the horizontal sync pulse and decreasing voltage narrows the pulse. A voltage above 2V sets the pulse on the horizontal sync-tip and increasing voltage narrows the pulse. At the boundary of the switchover between the two modes, there is a narrow region of uncertainty resulting in oscillation, which should be on problem in most applications. When there is no H-sync in sync-tip mode, the clamp pulse is generated by the VCO at the frequence preset by pin 6. This feature is intended for use in on screen display system.

Pin 3 Clamp pulse:
Active-low clamp pulse output.

Pin 4 Video Mute:

This open-collector output produces an active-low pulse when triggered by a step change of H-sync frequency.

Pin 5 F-Max:
A resistor from this pin to ground sets the upper frequency limit of the VCO.

Pin 6 F-Min:
A resistor from this pin to ground sets the lower frequency limit of the VCO.

Pin 7 VCC:
12V nominal power supply pin. This pin should be decoupled to pin 21 (GND) via a short path with a cap (C302) of at least 1000µf.

Pin 8 Vertical Sync In:
This pin accepts AC-coupled vertical sync of either polarity.

Pin 9 Composite Video In:
The composite video sync stripper is active only when no signal is present at pin 12 (H/HV In). The signal to pin 9 must have negative going sync tips which are at least 0.14V below black level.

Pin 10 H/HV Sync Out:
The sync processor outputs active-low H/HV sync derived from the active sync input (pin 9 or pin 12). Pin 10 stays low in the absence of sync input.

Pin 11 H/HV Cap:
A capacitor is connected from this pin to ground for detecting the polarity and existence of H/HV sync at pin 12.

Pin 12 H/HV Sync In:
This pin accepts AC-coupled H or composite sync of either polarity.

Pin 13 H Drive Duty Control:
A DC voltage applied to this pin sets the duty cycle of the horizontal drive output (pin 19). With a range of approximately 30%~70%. 2V sets the duty cycle to 50%.

Pin 14 H Drive EN:
A low logic level input enables H-Drive out (pin 19).

Pin 15 X-ray Shut Down:
This pin is for monitoring CRT anode voltage. If the input voltage exceeds an internal threshold. H-Drive out (pin 19) is latched high and video mute (pin 4) is latched low. Vcc has to be reduced to below approximately 2V to clear the latched condition, I.E power must be turned off.

Pin 16 Vertical Sync Out:
The sync processor outputs active-low vertical sync derived from the active sync input (pin 8, pin 9 or pin 12). Pin 16 stays low in the absence of sync input.

Pin 17 Vertical Cap:
A capacitor is connected from this pin to ground for detecting the polarity and existence of vertical sync at pin 8.

Pin 18 Flyback In:
Input pin for phase detecor 2. For best operation, the flyback peak should be at least 5V but not greater than Vcc. Any pulse width greater than 1.5µs is acceptable.

Pin 19 Horizontal Drive Out:
This is an open-collector output which provides the drive pulse for the high power deflection circuit. The pulse duty cycle is controlled by pin 13.

Pin 20 Horizontal Drive Ground:
Ground return for horizontal drive out. For best jitter performance, this pin should be kept separate from the system ground (pin 21), the respective ground traces should be met at a single point, located as close as possible to the power supply output.

Pin 21 Ground:
System ground. For best jitter performance, all LM1292 filter components and bypass capacitors should be connected to this pin via short paths.

Pin 22 Voltage Refer Cap:
This is the decoupling pin for the internal 8.2V reference. It should be decoupled to pin 26 (RETURN) via a short path with a cap (C301) of at least 470µf.

Pin 23 Phase Detector 2 CAP:
The low-pass filter cap for the output of phase detector 2 is connected from this pin to pin 26 (RETURN) via a short path.

Pin 24 Horizontal Drive Phase:
A DC control voltage applied to this pin sets the phase of the flyback pulse with respect to the leading edge of horizontal sync.

Pin 25 FVC CAP 1:
Primary FVC filter pin. Cfvc 1 is connected from this pin to pin 21 (GND) or pin 26 (RETURN) via a short path. The voltage at this pin is buffered to pin 27 (FVC out).

Pin 26 RETURN:
Ground return for the decoupling capacitor at pin 22 (Vref CAP), the filter capacitor at pin 23 (Phase Det 2 CAP) as well as the loop filter at pin 28 (PD1 OUT/VCO IN). This pin must be isolated from GND and H-drive GND.

Pin 27 FVC Out:
Buffered output of the frequency-to-voltage converter, which sets the VCO center frequency through an external resistor to pin 28. Care should be taken when further loading this pin, since during the vertical interval it presents a high output impedance. Excessive loading can cause top-of-screen phase recovery problems.

Pin 28 PD 1 Out/VCO In:
Phase detector 1 has a gated charge pump output which requires an external low-pass filter. For best jitter performance, the filter should be ground to pin 26 (RETURN) via a short path. If a voltage source is applied to this pin, the phase detector is disabled and the VCO can be contorlled directly.

3.2.3. IC302 LM1295 DC Controlled Geometry Correction System

The LM1295 is specifically designed for use in a continuous sync monitor. The injection-locked vertical oscillator operates from 50 Hz to 170 Hz, covering all known video monitors. A differential ouptut current is provided in order to prevent ground interaction.

The IC302 provides two outputs composed of the summation of DC controlled 1st and 2nd order ouptut terms. The first ouptut corrects for EW pincushion and trapezoid. The second corrects for parallelogram and bow.

A DC controlled output is provided for vertical dynamic focus correction.

3.2.4. IC302 LM1295 Pin Descriptions

Pin 1 Ground:
This pin should be connected to the power ground at pin 17.

Pin 2 Vertical Height:
A Voltage between 0V and 4V on this pin controls the amplitude of the +V and -V drive currents, with increasing voltage giving increasing current. The control range is approximately 1.8 to 1. The response time is low, being limited by the automatic level control loop.

Pin 3 4V CAP:
A C202 capacitor aluminum electrolytic or tantalum, should be connected between pin 3 and GND to bypass the internal 4V reference.

Pin 4 Vertical Sync In:
The vertical sync input takes a negative-going TTL level pulse which injection locks the vertical oscillator to the vertical sync frequency if it is above the LM1295 minimum frequency. The minimum pulse width is approximately 200µs. For free-running detection (no vertical sync in), this input should be at logic high.

Pin 5 8V CAP:
A C203 capacitor, aluminum electrolytic or tantalum, should be connected between pin 5 and GND (pin 17) to bypass the internal 8V reference.

Pin 6 Vertical Dynamic Heigh:
A voltage between 3V and 4V on this pin controls the amplitude of the +V and -V drive currents with increasing voltage giving increasing current. The control range is approximately 1.3 to 1.

Pin 7 Vcc:
Vcc should be bypassed to GND (pin 17) with a C216 aluminum electrolytic or tantalum capacitor. The supply voltage is 12V.

Pin 8 Voltage Reference CAP:
A C217 capacitor aluminum electrolytic or tantalum, should be connected between pin 8 and GND (pin 17).

Pin 9 Horizontal Dynamic width:
This output consists of the sum of the vertical ramp and the parabola derived from the ramp. The amplitude and polarity of the ramp signal is DC controlled by horizontal trapezoid control (pin 11) and of the parabola by E-W pin control (pin 10). The weighting of lthe ramp is 1/3 the parabola; i.e, with the horizontal trapezoid and E-W pincushion controls at 4V, the output is 3 parts parabola and 1 part ramp. Horizontal dynamic width is used to correct for trapezoid and east-west pincushion distortion.

Pin 10 E-W Pincushion Control:
A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the horizontal dynamic width (pin 9) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitude increases and the parabola is negative-going.

Pin 11 Horizontal Trapezoid Control:
A voltage of 0V to 4V adjusts the polarity and the amount of vertical ramp in the horizontal dynamic width (pin 9) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the ramp is positive-going. From 2V to 0V, the amplitude increases and the ramp is negative-going.

Pin 12 Horizontal parallelogram control:
A voltage of 0V to 4V adjusts the polarity and the amount of vertical ramp in the horizontal dynamic center (pin 14) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the ramp is positive-going. From 2V to 0V, the amplitude increases and the ramp is negative-going.

Pin 13 Horizontal Bow Control:
A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the horizontal dynamic center (pin 14) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitude increases and the parabola is negative-going.

Pin 14 Horizontal Dynamic Center:
This output consists of the sum of the vertical ramp and the parabola derived from the ramp. The amplitude and polarity of the ramp signal is DC controlled by horizontal parallelogram control (pin 12) and of the parabola by horizontal bow control (pin 13). The difference between this output and the horizontal dynamic width output is in the weighting of the ramp, which is equal to the parabola; i.e with the horizontal parallelogram and horizontal bow controls at 4V, the output is 1 part parabola and 1 part ramp. Horizontal dynamic center is used to correct for parallelogram and bow distortion.

Pin 15 Vertical Dynamic Focus Control:
A voltage of 0V to 4V adjusts the polarity and the amount of parabola in the vertical dynamic focus (pin 16) output. At approximately 2V, the amount is zero. From 2V to 4V, the amplitude increases and the parabola is positive-going. From 2V to 0V, the amplitue increases and the parabola is negative-going..

Pin 16 Vertical Dynamic Focus:
This output consists of the parabola derived from the vertical ramp. The amplitude and polarity are controlled by vertical dynamic focus control.

Pin 17 Ground:
This is the power supply ground for the 12V supply and the point to which the bypass capacitors are returned.

Pin 18 Automatic Level Control CAP:
This capacitor (C204) is part of the level control circuit that maintains constant vertical height in spite of vertical sync frequency changes. If the VCO capacitor value is changed, the capacitor value should change in the same ratio. A R204 resistor should be connected from this pin to ground.

Pin 19 Double Frequency Capacitor:
This capacitor (C218) prevents the vertical oscillator from locking at twice the vertical sync frequmcy. If the VCO capacitor volue is changed, this capacitor value should change in the same ratio.

Pin 20 Oscillator Capacitor:
This is the vertical oscillator capacitor (C232). The value can be changed to change the minimum frequency.

Pin 21 Vertical Resistor:
One end of the vertical resistor connects to this pin. This resistor determines the gain of the vertical ramp current generator. The gain is inversely proportional to the resistance.

Pin 22 Vertical Resistor:
The other end of the vertical resistor connects to this pin.

Pin 23 Vertical Drive:
This is the negative-going vertical ramp output current of the differential pair. The ramp current waveform is superimposed on a direct current of approximately 315µA. The waveform amplitude is determined by the vertical height (pin 2) control voltage and the vertical dynamic (pin 6) control voltage. The current can be converted into voltage by a R236 resistor to ground or by a differential amplifier using the differential currents as inputs. The voltage compliance of the output is typically 6V.

Pin 24 + Vertical Drive:
This is the same as vertical drive except it is the positive-going output current of the differential pair.

3.2.5. Vertical Deflection Circuit

1. IC201 TDA8172 consists of a flyback generator, voltage stabilizer, drive circuit and vertical output amplifier.
2. **The vertical oscillator circuit**

   (a) The frequency and phase of the vertical oscillator circuit is generated by the vertical synchronization signal.

   (b) The synchronization signal is input from Pin 4 of IC302 LM1295, and after being processed by the synchronization circuit, is sent to the vertical synchronization oscillator circuit to trigger the vertical oscillator and synchronize the oscillator frequency with the external synchronization signal. The frequency of its internal free oscillation is set by the time constant of C232. It does not need an external F/V control because this IC302 can keep vertical synchronization. Pin 18 provides vertical A.L.C function. So the pin 18 of IC302 is use to maintain the difference between the free oscillation frequency and external synchronization signal frequency at a similar level and make the sawtooth wave amplitude from pin 24 of IC302 the same.
3. **Vertical Size Control**

   The pulse voltage output by the oscillator is sent to the sawtooth wave generator. The size and amplitude of the voltage of the sawtooth wave generation can be changed by DC value which output from Pin 35 of IC801 (PWM) and the vertical size can thus be controlled. This sawtooth wave voltage passes through a buffer and is output from Pin 24 of IC302 to pin 1 of IC201 TDA8172 of the vertical drive circuit.

   The vertical ramp and DC offset are also controlled by PWM output. The vertical ramp gen-

erated across C232 is buffered internally to IC302 by DC controlled variable gain stage. The voltage level is derived from pin 35 of IC801 (PWM) through the R210, R206 and C206 of grneration, then into pin 2 of IC302.

4. **Vertical Drive Circuit**

(a) It is not sufficient to rely solely on the oscillator circuit output to ensure the stability of the vertical output, so a first or second level amplifier circuit must be inserted between the oscillator circuit and the output. This circuit is called the drive amplifier and in addition to amplifying the sawtooth wave also corrects the vertical linearity.

After adding the drive circuit, because the level of amplification can be considerable, enough negative feedback can be added to correct vertical linearity and increase the stability of the circuit.

(b) If the current of the sawtooth wave flowing through the deflection yoke is distorted, then the top and bottom portions of the display will be expanded or compressed, resulting in poor linearity. In order to solve this problem, correction of the linearity of the sawtooth wave can be carried out before the drive level.

5. **IC201 TDA8172 Vertical Drive Circuit**

The IC201 uses a double power source, so it can be viewed as an OCL drive amplification circuit.

In order that the DC coupled output stage accurate DC reference, a DC reference voltage is taken from pin 5 of IC302. This used as the reference voltage (via divider resistors, R214) for the DC coupled power amplifier IC201. This is a simple voltage to current inverting amplifier, using R223 to derive a voltage proportional to the current in the deflection winding of the yoke. This voltage is fed back to the virtual signal earth inverting input of the power amplifier(pin1) by R219. This back to back diode feedback network modifies the linearity of the transfer characteristic in order to give precept "S" correction linearity, in addition to the variable correction in the ramp generator.

The vertical output amplifier has a voltage boost circuit to triple the positive supply voltage during retrace in order to speed up flyback. It does this by charging capacitor C210 through diode D202 during the normal forward scan. Pin6 of the IC201 is the voltage supply to the power output stage. When flyback occurs, pin3 is switched to the positive supply rail on pin2, thus adding the voltage across C210 to that of the supply rail, effective doubling the supply momentarily.

6. **Vertical Centering Adjustment**

Since IC201 functions as an OCL circuit, VDC is output from Pin 7 of IC201, so the central current can be changed to shift the on-screen display up or down to prevent voltage fluctuation. The DC operating point of the amplifier can be varied by the pin 38 of IC801 (vertical position) output and via R212, C207 and R213 to pin 7 of IC201 which adds or subtracts an offset into the output, thus varying the DC offset of the scan and hence the vertical centering.

3.2.6. Geometry Correction Circuit

1. If the width of the border in the center of the screen is insufficient, the waveform shown in Figure 3-3 below, can be used to add to horizontal deflection B+ in order to change the deflection of the horizontal deflection circuit. This waveform is the parabola obtained after regulation of the vertical period, and is created to perform amplitude modulation on the horizontal deflection current, as shown in Figure 3-4.

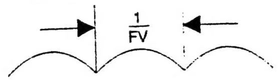


Figure 3-3 Voltage Correction Wave

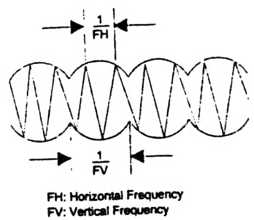


Figure 3-4 Current Correction Wave

2. The sawtooth wave is output from Pin 9 of IC302 and through C350 and R364 and input to Pin 2 of IC601 (DC to DC circuit). It is then output from Pin 6 of IC601 and after being sent to T603's second coil output, is added to horizontal B+ to provide pincushion and trapezoid distortion correction. So, is created to preform amplitude modulation on the horizontal deflection output pluse, as shown in figure 3-5.

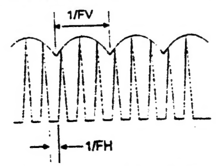


Figure 3-5 Collector of Q303 Output Pluse Correction Wave

3. The sawtooth wave is output from pin 14 of IC302 and through R353 and C314 and input to pin 24 of IC301. It is added to horizontal phase to provide parallelogram and bow distortion correction.

3.2.7. Structure of Horizontal Deflection Circuit

The function of the horizontal deflection circuit is to cause left/right scanning of the electron beam using the sawtooth wave current flowing through the horizontal deflection yoke, and is made up of the horizontal oscillator circuit, horizontal drive circuit, horizontal output circuit, synchronous AFC circuit and high voltage generator circuit.

1. **Horizontal Drive Amplifier**
In order to rapidly saturate the output transistor (ON) or cut it off (OFF), a sufficient basic current must be provided. Because of this, an amplifier circuit is added between the oscillator circuit and the output circuit to amplify the pulse voltage. At the same time, after the waveform has been regulated, by adding this circuit to the output circuit, this amplification circuit functions as a drive amplifier.

IC301 LM1292 consists of a vertical sync selection polarity circuit, composite video sync stripper circuit, AFC circuit, H/V sync and composite sync circuit, voltage control oscillator circuit, phase regulator circuit, X-Ray circuit, video mute circuit, voltage regulator circuit and horizontal drive duty cycle circuit. This IC includes the vertical and horizontal circuits combined in one package.

When the synchronization signal input to logic circuit and pin 12 of IC301. The pin 19 of IC301 output horizontal frequency is achieved by the pin 1 of IC801 and flyback pulse from between C380 and C381 fed to pin 18 of IC301. So, the pin 19 of IC301 output horizontal frequency through Q311, Q312, Q302, Q104 T101 and T301 provide a horizontal output transistor base current of Q303 and horizontal anode voltage generator output transistor base current of Q105.

The horizontal output transistor base drive is taken from a conventional base drive transformer stage. This circuit as in a similar manner to a flyback power supply. The square wave horizontal oscillator output signal is coupled into the base of emitter drive stage transistor Q302, Q104, T301, T101 across the +15V supplies. This causes the primary current to increase linearly until such time as Q302 and Q104 turns off, hence storing a predetermined amount of flux energy in the transformer. As Q302 or Q104 turns off, and the primary current falls to zero, the secondary voltage is driven above the threshold of the base-emitter junction voltage of the horizontal output transistor Q303 or Q105. Current flows through R320, R321, L301, L302 and D303 into the base of Q303 or through R116, R117, L101 and D130 into the base of Q105 hence turning this device on. The high base current of around 1.1A. Lamps is so high that Q303 or Q105 is driven heavily into saturation. This is important in order that the collector voltage should be as low as low as possible whilst conducting the high peak currents that flow through the horizontal deflection winding. In turn, this is vital to limit dissipation.

At the required time as determined by the horizontal oscillator, the base drive transistor is turned back on. The voltage at Q302 or Q104 collector fall rapidly back towards the ground rail. However, the secondary current still remains flowing in a positive direction for a short time, due to the finite leakage inductance of T301 or T101. Also, due to the heavy saturation of Q303 or Q105, the base voltage remains at around 1V. The current in the secondary winding rapidly reverses and goes sharply negative as the charge stored within the base region of Q303 or Q105 is removed. D303 or D130 helps to speed up this charge removal. Note that during this time, the collector output of the Q303 or Q105 is still turned on, even though the base current is flowing out of the base.

This period of time is known as the storage time of the device and may take between 2-3us, depending upon peak collector current and temperature and various other design factors. Finally, when all charge in the base region of Q303 or Q105 is dissipated the base current suddenly stops, and the secondary current drops almost instantly to zero. At that point, the device now become non conducting and the collector current flow also terminates. The secondary voltage on T301 or T101 drops to it's unloaded voltage and the current flow in the primary settles to it initial value once more.

2. **Horizontal Equivalent Output Circuit**
The horizontal output circuit uses the switch operation of a transistor and a damping diode, and provides a sawtooth wave current to the deflection yoke. The horizontal deflection yoke is made up of the L value on the coil and resistance r inside the coil connected in series. Its resistance is extremely small, and the time constant (L/r) is extremely large. Because of this the voltage at the two terminals of the coil cause rapid variation in the current flowing in the coil still will slowly vary, creating a sawtooth current. The basic circuit and equivalent circuit are shown in Figures 3-6 and 3-7.

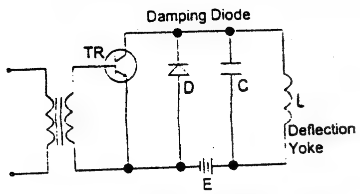


Figure 3-6 The Basic Deflection Circuit

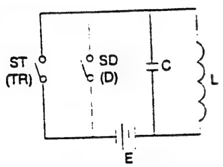


Figure 3-7 Equivalent Circuit

3. **Horizontal Output Equivalent Circuit Operation**

Refer to Figure 3-8 for the current wave of the voltage of the horizontal output circuit during operation.

(a) t1 — t2 Period

The base of the output transistor is added to the forward bias voltage. As the current through the base is very large, it will cause the output transistor to be saturated, corresponding to the ON state of S1 in the equivalent circuit. At this time the deflection yoke contains a current flow and because the time constant is large, the current will slowly show a linear increase as shown in Figures 3-8 (b) and 3-9 (a).

(b) t2-t3 Period

At t2, a negative load is applied to the to the base and the output transistor changes to OFF (S1 in open state). There is no current passing through the transistor at this time and the L and C components of the deflection yoke become

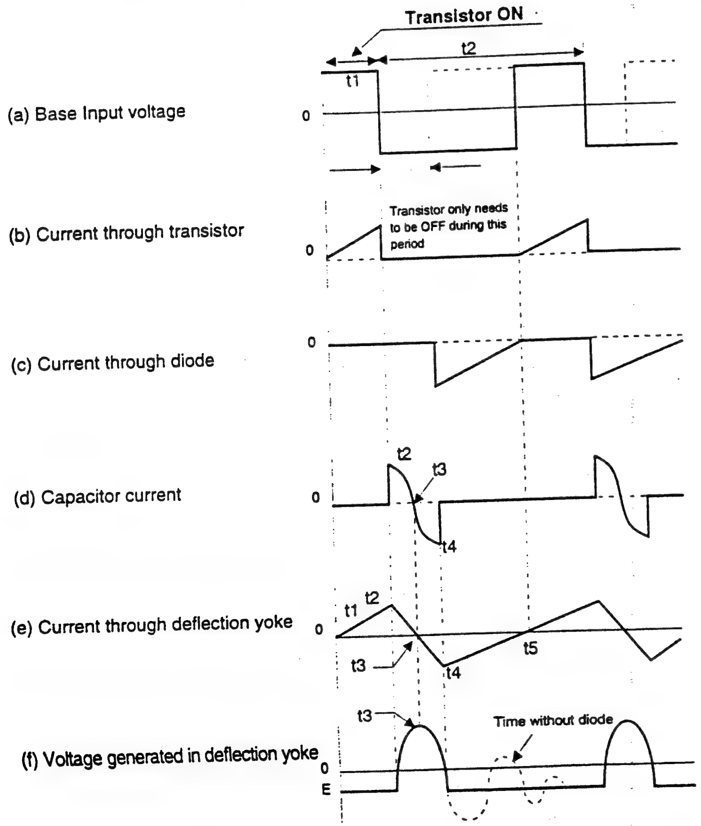


Figure 3-8 Horizontal Output Voltage/Current Waves

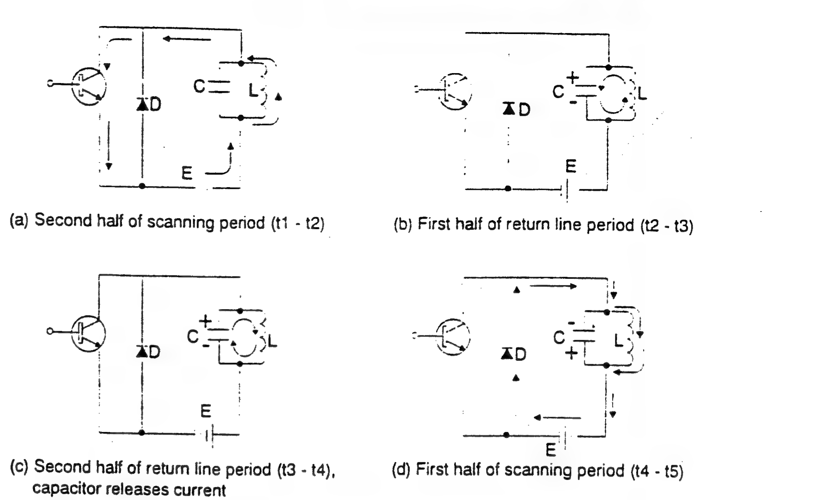


Figure 3-9 Polarity of Transformer Voltage

independent oscillation circuits. If the current is suddenly cut off, then the polarity of the inverse voltage generated at L will be as shown in Figure 3-9 (b). This voltage is viewed as the source voltage and will cause current to flow, at which time the current flowing to C is as shown in Figure 3-8 (d). At time t3 this current is 0 but the voltage at the two capacitor terminals is at maximum. This waveform is known as flyback pulse, and is shown in Figure 3-8 (f).

(c) (t3 — t4) Period

The energy accumulated in C is released to the deflection yoke, the direction of the current flow being shown in Figure 3-9 (c). The current increases as the voltage on C decreases, and at time t4, the voltage of C is 0, at which time the current is at maximum, which means the current flowing into the deflection yoke is also maximum. C is then charged and if a damping resistor is not connected, the energy between L and C will be reversed, which is the oscillation frequency set by the oscillator at L and C.

(d) t4 — t5 Period

At t4, the voltage of C is 0. After this it is recharged in the opposite direction and this voltage exceeds the voltage of the power source at time t4. At this time the damping diode is ON and the L and C circuits are shorted out and stop oscillating. Because of this the time constant of r and L in the damping diode is large so the current flowing in the deflection yoke does not suddenly become 0. The current shows a linear decrease, and when it becomes 0 at time t5 the transistor is ON and the operation described above is repeated.

As described above, the current flowing in the deflection yoke during scanning is the sum of the current which has passed through the transistor and the damping diode current. Please refer to Figure 3-8 (e).

4. **Horizontal output operation:**

The actual output stage differs from the simple model described in a number of ways. Refer to the basic schematic of the major components in Figure 3-10.

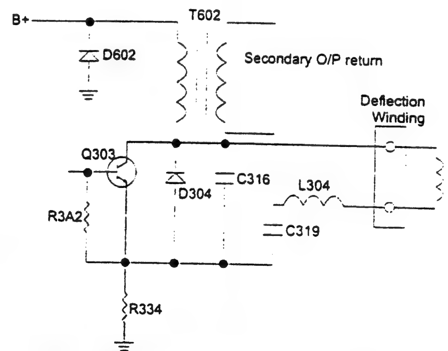


Figure 3-10 Basic Horizontal Deflection Output Circuit

The main inductance L is now divided into the primary winding of the Flyback Transformer (FBT) T602 and the deflection yoke winding. The deflection yoke is coupled through a capacitor C319, which has two function. Primarily it prevents DC unwanted DC currents

flowing through the deflection yoke which would otherwise cause an undesirable deflection of the CRT beam.

Secondly, the voltage drop across it due to the AC ramp current flowing causes a parabolic modulation in the slope of the ramp, leading to a progressive curve in the ramp, symmetrical about the zero current value as shown in Figure 3-11. This intentional distortion of the linear ramp is required to compensate for the 'S', or symmetric linearity distortion in the CRT.

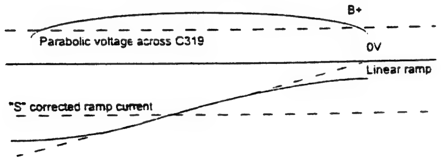


Figure 3-11 Linear Ramp Distortion

In series with C319 and the deflection yoke is another indicter, L304. This is a saturating indictor that is biased with a permanent magnet. Consequently this device has a linearity that is higher for current flow in one direction than in the opposite direction. This function provides compensation for resistive losses that would otherwise cause an undesirable exponential curve to the linear ramp, resulting in asymmetrical linearity errors in the displayed image.

The voltage seen in the output stage require special attention. The B+ supply can varying between 60-180V. The main flyback pulse seen across Q303 and associated components is around 1100Vp. Consequently, appropriate precautionary measures must be taken when servicing the monitor.

In addition to the basic topology as described above, there are a number of other additional devices. Q306, Q307, Q330 and Q333 can be independently turned on or off under logic control. These devices switch addition capacitors, C320, C322, C362 and C367 in parallel with C319 to alter the amount of 'S' correction at different horizontal scan frequencies.

D308 and D309 acts as a constant current source that can be under SW301 and SW302 control. This current source drives an adjustable constant current into L304. This current flows into the deflection yoke and adds a variable DC offset to allow image raster centering to be achieved.

The B+ provides current for the deflection coil (D/Y). Therefore, changes in deflection current can be controlled by modifying B+ voltage. As a result, horizontal width can be modified. In order to obtain the side horizontal width for different frequencies, a DC to DC feedback circuit is added. The synchronization signal comes from deflection output, from between C380 and C381 to base of Q603 which drives Q604 to trigger pin 4 of IC601. Feedback signal come from secondary on T601, via D604, R621 and R611 to become a DC voltage on pin 2 of IC601, another feedback signal passes through emitter of Q303, via R606 on pin 3 of IC601. There signals determine duty cycle of output signal of IC601 which is coupled to T603 to drive Q601, to control B+, making it possible to have correct deflection current and horizontal width on different frequencies. Similarly, output pin 30 and pin 31 of IC801 drive through R368, C348, R369, R366, C347, R367 and R610 to control duty cycle of IC601 output to achieve horizontal width adjustment.

During mode change, the B+ supply can be instantly turned off by pulling up the error amplifier input on pin 1 of IC601. These can be achieved by Q602, Q606 and Q605 which is driven from the logic circuit pin 9 of IC801 (MUTE). Whilst Q602, Q606 and Q605 can switch off the B+ supply almost instantly, the time taken for the supply to restart is programmed by the value of logic circuit.

In addition, the B+ (215V) supply is configured so as to maintain a constant anode voltage. The anode voltage is derived from the flyback transformer T103. As the flyback voltage across the primary is already a high voltage pulse of around 680Vp, it requires only a modest turns ratio to step this pulse up to around 27kV, the working voltage of the CRT. Refer to the basic schematic of the major components in figure 3-12.

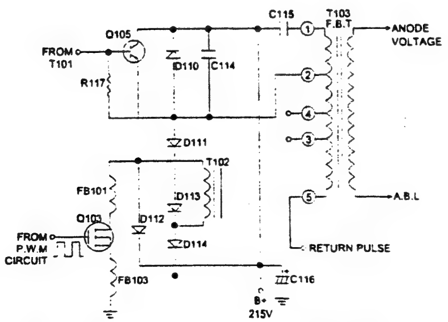


Figure 3-12 Basic High Voltage Output Circuit

The flyback pulse at the primary of T103 is proportional to the both frequency and the supply rail B+. In order to maintain the anode voltage at a constant 27kV a regulation system is required. This is achieved using a PMW regulation stage formed by a IC101 driving a Q103. The causes a regulating current on primary T102, the voltage changes in secondary T102 result in a constant high voltage, synchronized by the horizontal oscillator. The IC101 has an error amplifier that generates an error signal from the feedback network formed by the high voltage bleed resistor and capactior (it is internal to T103). Resistors VR101, R103 and R104 set the DC feedback ratio, and by adjustment of VR101, this ratio can be adjusted at setup to set the high voltage at it's nominal value of 27kV. The AC frequency response of the serve loop is set by C104 and R114 for optimum stability and relegation characteristics.

The output of the error amplifier which can be observed on pin 1 of IC101 is internally compared with a DC voltage. This DC is produced across.

The average beam current through the CRT also flows through the secondary high voltage winding of T103 connected to pin 8 of T103. C132 and R138 smooths the pulse of current flowing in the secondary winding and the average DC current is supplies through a variable resistor VR106. When the average secondary current flowing exceed 460mA, this voltage begins to drop below this threshold. Thus a signal is generated which can be fed to video amplifier for automatic beam current limiting (ABL).

3.2.8. X-RAY Protection Circuit

The feedback pulse voltage from T103 F.B.T is regulated through D302 to obtain a DC voltage and the appropriate set voltage is distributed by R323 and R324. When the feedback pulse voltage exceeds the set voltage, a DC voltage develops in the cathode of ZD302 which turns on Q304 and Q305. As a result, the pin 1 of IC306 (adj-pin) to 0V, so IC306 is turned off, putting the 12V is not output. This is the phenomenon of high voltage protection.

3.2.9. The Focus Circuit

The output waveform come from pin 16 of IC302 through C122 and R123 to the amplifier Q106, via T104 with horizontal waveform to modulation. After, the wave coupling of the T103 which make the focus performance on the C.R.T. This is waveform shown in figure 3-13.

3.2.10. Horizontal linearity and CS Switching

Switching CS is necessary to ensure the lines are in accordance with the specifications in multi-sync monitors.

- For frequencies 79~95kHz, CS is only C319.

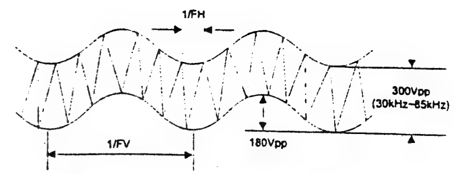


Figure 3-13 Focus Correction Wave

- For frequencies 68~79kHz, CS are C319 and C362.
- For frequencies 55~68kHz, CS are C319 and C322.
- For frequencies 49~55kHz, CS are C322, C319 and C362.
- For frequencies 43~49kHz, CS are C320 and C319.
- For frequencies 41~43kHz, CS are C320, C362 and C319.
- For frequencies 37~41kHz, CS are C320, C322 C362 and C319.
- For frequencies 35~37kHz, CS are C319, C320 C362 and C367.
- For frequencies 30~35kHz, CS are C319, C320 C322, C362 and C367.

Truth Table of Frequency Discriminator

CS / FEQ	CS1	CS2	CS3	CS4	DP5
30~35 kHz	L	L	L	L	L
35~37 kHz	L	H	H	L	L
37~41 kHz	L	L	L	H	L
41~43 kHz	L	H	L	H	L
43~49 kHz	L	H	H	H	L
49~55 kHz	H	L	L	H	L
55~68 kHz	H	L	H	H	L
68~81 kHz	H	H	L	H	L
81~95 kHz	H	H	H	H	H

Truth Table of Power Saving Detector

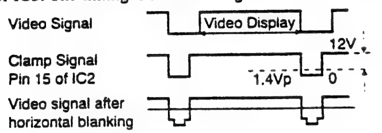
Mode	H-sync	V-sync	PMG1	PMG3	Mute	Blanking
ON	Pulse	Pulse	1	0	0	0
Standby	No Pulse	Pulse	1	1	1	1
Suspend	Pulse	No Pulse	0	1	1	1
OFF	No Pulse	No Pulse	0	1	1	1

3.3. Video Amplifier

The RGB video and sync signals are supplied through a video cable directly to the Video Board at connector P1. The RGB signals are terminated in 75 ohms by R51, R31 and R1.

The RGB signals then enter an IC3 LM1282 video pre-amplifier, providing synchronous black level clamping, variable picture contrast (gain) and RGB gain balance for alignment. Separate gain control voltages for the three pre-amplifier channels are provided via R67, R47 and R17 from the IC5 M62393 DAC which is loaded by the microcontroller via the I2C bus. These inputs enable the individual gains of each channel to be varied to allow channel gain balance. In addition, a common signal is applied on pin13 of IC3 to adjust all three channels by the same amount, to allow for overall gain or contrast control.

A synchronous clamping signal is derived from the horizontal sync pulse by Q2. This takes the trailing edge of the horizontal sync pulse, differentiates it through C74, which is applied pin 15 of IC3. The timing is shown in Figure 3-14.



NOTE:
A. Clamp signal is generated from horizontal sync pulse time.
B. When the Clamp signal is less than 1.4Vp-p, the IC's internal clamp loop will operate; when greater than 1.4Vp-p, it will not operate.

Figure 3-14 Timing of Pin 15 Clamp Signal

The outputs of the video pre-amplifier are fed to IC1, a hybrid power amplifier IC type VPS12, through resistors R56, R36 and R6. In addition, on screen display video information generated by IC1 can be through pin 2, pin 8 and pin 12 of IC1.

IC2 is an on screen display processor. This is a simple video generation IC2 that has its own oscillator circuit, the oscillator circuit by using an internal Phase Locked Loop (PPL) the IC2 can sync to the incoming vertical and horizontal oscillator frequencies and produce the OSD video signals once initialized and loaded by the commands and data received on the I2C bus. When the OSD display is activated, the blanking output of the IC2 also sends a signal to the blanking input of IC3 (pin 16) to provide an optional black background for the OSD display.

The RGB signals are amplified to drive the CRT by an IC1 VPS12 hybrid amplifier and capacitively coupled to the cathodes. Brightness control is achieved by varying the bias of G1 of the CRT via a transistor stage formed by Q111 which is also driven by an output of the pin 12 of IC5.

IC1 amplifies the video signals to around 40Vp-p. The outputs are AC coupled to the CRT cathodes via C9, C39 and C59. In order to bias the DC level of the cathodes correctly, the AC coupled signal is DC restored by clamping to a DC voltage which can be varied under microprocessor control. Considering Red channel output on IC1 as an example, the signal is clamped by D4 to the voltage set by the transistor amplifiers formed by Q3, which amplify the adjustable voltage at the output of the DAC. A similar stage can be seen for the green and blue channel outputs.

When the RC video signal amplification circuit is added for amplification, this waveform will change as shown in Figure 3-15 (a). Without the DC component, as shown in Figure 3-15 (b), the DC level of darker and brighter displays will be different, so when this kind of signal without a DC component is sent to the CRT, it will cause the contrast of the image to change as the signal changes. Therefore Q3, Q33, Q53, D4, D34 and D54 serve as a DC clamp and the CRT's cathodes DC voltage can be adjusted by the pin 12, pin 13, pin 14 of IC5 M62393 DAC.

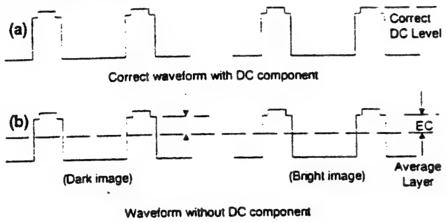


Figure 3-15 The Post Output Amplifier Circuit

IC2 is an On Screen Display processor. This is a simple video generation IC2 that has its own oscillator circuit. The oscillator circuit by using an internal Phase Locked Loop (PLL) the IC2 can sync to the incoming vertical and horizontal oscillator frequencies and produce the OSD video signals once initialized and loaded by the commands and data received on the I2C bus. When the OSD display is activated.

The RGB signals are amplified to drive the CRT by an IC1 VPS12 hybrid amplifier and capacitively coupled to the cathodes.

Brightness control is achieved by varying the bias of G1 of the CRT via a transistor stage formed by Q111. Vertical blanking signals is coupled into this amplifier Q204, Q205 and Q202 to prevent visible retrace lines.

3.4. Microprocessor And Sync Processing

The microprocessor is a MC68HC705BD9B type. It is particularly suitable as multisync computer monitor controller. This 8-bit microcontroller unit (MCU) contains an onchip oscillator, CPU, RAM, ROM, M-Bus serial interface system (IIC), parallel I/O, Pulse Width Modulator, Multi-Function Timer and sync Signal Processor. It has a 24.76k bytes of ROM and 384 bytes of RAM on internal which contains a basic communication 'boot' routine and various other simple routines. It is also used to store the OSD icon bit map. The main firmware routines and variable data stored in the 16k external EEROM, IC802.

When the micro is instructed via the I2C bus, the internal ROM boot routine will load up the EEROM with program data from the I2C bus. Thus it can be made to load its own

firmware. From then on it will run jointly out of EEROM and internal ROM. Another important routine within the internal ROM is the routine which allows data writes to be made to the EEROM. This must be resident in the micro as it cannot run from the EEROM whilst writing data. These control the addressing and I/O port selection from the micro CPU in the IC801 (MC68HC705BD9B).

Also specialized ports Pin36, Pin 37, Pin 38 and Pin39 of IC801 form the M-Bus interface which is used internally to set the DAC valuse. Other way, specialized ports pin 11 and pin 12 of IC801 from the M-bus interface which is used internally to set the data to external EEROM IC802. In addition, the I/O ports from pin 40, pin 41 of IC801 from the M-bus interface which is used internally to set the front panel control.

There are 14 PWM channel. It can be made to control H-PHASE, PARALLELOGRM, PIN-BALANCE, TRAPEZOID, PINCUSHION, TILT, V-SIZE, H-SIZE and V-POSITION on the pin 19 to pin24, pin 28 to pin 35 of IC801.

The micro also drives the sync selection circuits. IC801 is used to set the polarity of the incoming sync signals and allows the micro to sample the vertical and horizontal syncs and to select the correct polarity on the outputs H-SYNC and V-SYNC appropriately. In addition, whilst sampling the polarity, the micro can measure the frequency of both syncs. By suitable selection of H-SYNC and V-SYNC control lines, it does this when ever a mode change occurs. A mode change is detected by either a change in vertical frequency, which is monitored by firmware, or by a sudden change in horizontal frequency.

When power is disturbed to the unit, the power reset line goes low. This also causes an input to the micro via the MODEC line. On detecting this interrupt, the micro first checks inputs Pin 2 of IC801. If these are also low, then it knows the MODEC interrupt was caused by an impending power failure. In this case the micro saves the current RAM data in EEROM and prepares for power off. The RESET line is delayed for 7ms by R801, ZD801, R803 and C801 to allow time for the data to be saved. The REST line then holds off the micro and the EEROM until power is good once more.

Notes

Section 4.

Setup Adjustments

4.1. Preparing the Display for Adjustment

Before adjusting any the display settings or making final adjustments after service, perform the following pre-test settings to prepare the display for adjustment:

1. Be sure to allow the display to warm up for at least 30 minutes before making any adjustments.
2. When making tests and adjustments, the CRT should be facing east or west to minimize the affect of the earth's magnetic field.
3. Set the contrast control at 80% and the brightness control at 50% for all tests unless otherwise specified.
4. Thoroughly degauss the entire screen with a manual degausser before proceeding with tests.
5. All test should be performed with the rated power supply voltage unless otherwise specified.

4.1.1. Test Equipment Required

The following equipment will be required to make the tests and adjustments detailed in this section:

- ☐ Video signal and pattern generator
- ☐ Digital multimeter
- ☐ Degausser

4.2. Adjustment Procedures

4.2.1. Adjustment Sequence

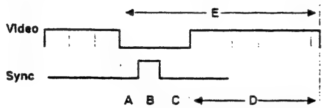
This display undergoes an automatic alignement procedure during manufacture. This alignment procedure follows a fixed sequence of adjustments which are dupplicated in this section. When making manual adjustments during service, you should always make the adjustments in the order given here to ensure correct results.

4.2.2. Preset Timings Used During Adjustment

During alignment it is necessary to input certian preset timings stored in the display. The detailed parameters of all the preset timings are given in the table below for your reference.

IMPORTANT NOTE

The preset timings for different versions of this model may differ from those shown here. Be sure to check the list of preset timings for the unit being serviced.



Mode Number	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7	Mode 8	Mode 9	Mode 10
Data Pixel	640	640	1024	1152	1280	800	800	1024	1280	1600
Data Line	400	480	768	864	1024	600	600	768	1024	1200
H. Freq.(kHz)	31.469	31.469	60.023	67.500	79.976	46.875	53.674	68.667	91.146	93.750
V. Freq(Hz)	70.087	59.942	75.029	75.000	75.025	75.000	85.061	84.997	85.024	75.000
Pixel Rate(MHz)	25.175	25.175	78.750	108.000	135.000	49.500	56.250	94.500	157.5	202.50
Hor. FP µs(A)	0.636	0.636	0.203	0.593	0.119	0.323	0.569	0.508	0.406	0.316
Hor. Sync µs(B)	3.813	3.813	1.219	1.185	1.067	1.616	1.138	1.016	1.016	0.948
Hor. BP µs(C)	1.907	1.907	2.235	2.333	1.837	3.232	2.702	2.201	1.422	1.501
Hor. Active µs(D)	25.422	25.422	13.003	10.667	9.481	16.162	14.222	10.836	8.127	7.901
Hor. Total µs(E)	31.778	31.778	16.660	14.815	12.504	21.333	18.631	14.561	10.971	10.667
Ver. FP ms(A)	0.381	0.318	0.017	0.015	0.013	0.021	0.019	0.015	0.011	0.011
Ver. Sync ms(B)	0.064	0.064	0.050	0.044	0.038	0.064	0.056	0.044	0.033	0.032
Ver. BP ms(C)	1.112	1.048	0.466	0.474	0.475	0.448	0.503	0.524	0.483	0.491
Ver. Active ms(D)	12.711	15.253	12.795	12.800	12.804	12.800	11.179	11.183	11.235	12.800
Ver. Total ms(E)	14.269	16.683	13.328	13.333	13.329	13.333	11.756	11.765	11.761	13.333
Polarity(H.V)	-,+	-,-	+,+	+,+	+,+	+,+	+,+	+,+	+,+	+,+
Primary mode is 91.146kHz / 85.024Hz (1280x1024)										

Table 4-1 Table of preset Timing Parameters

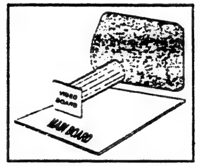
IMPORTANT NOTE

The adjustment settings in this section are based on REVISION B of the factory alignment procedures. Appendices detailing changes in the factory alignment procedures that have occurred since publication of this service manual are available upon request.

Initial settings to be carried out manually prior to automatic alignment:

4.3. High Voltage Verification

1. Input a cross hatch pattern in 93.75KhZ (1600X1200) mode and adjust VR101 on the main board (see figure 4-1 for approximate location) so the high voltage is in the range 28kV~30kV the set will shut down.
2. Input a full white pattern in 31.47kHz (640x400) mode, check that the high voltage is in the range 26kV±0.3.



Location of PCBs

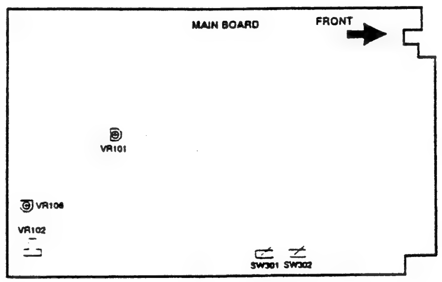


Figure 4-1 Location of on Main board

4.4. G1 Voltage Adjustment

Input a raster pattern (video OFF) in primary mode and push the external brightness control button to maximum. Adjust VR102 (see Figure 4-1 for approximate location) so that the voltage of G1 read on a digital multimeter is -30V±1.

Steps used in white balance adjustment:

4.5. Background Brightness Setting

1. Input a raster pattern in primary mode and push the external brightness control button to maximum. Adjust the SCREEN VR so background brightness is approximately 1.0FL±0.1.
2. Before carrying out white balance adjustment, make sure that the display size and linearity are in spec.
3. Before carrying out white balance adjustment, make sure that the VR106 (see Figure 4-1 for approximate location) position shall be turn counterclockwise to the end (ABL no action).
4. Input timing in primary mode, and the white balance automatic adjust some item as blow.
   a) Input no video pattern in primary mode, and set-up brightness of raster white balance get the x,y value is x=0.346±0.01 y=0.359±0.01.
   b) Input a full white pattern in primary mode, and set-up 5000 degrees kelvin of picture white balance get the x,y value is x=0.346±0.01 y=0.359±0.01.
   c) Input a full white pattern in primary mode, and set-up 6500 degrees kelvin of picture white balance get the x,y value is x=0.313±0.01 y=0.329±0.01.
   d) Input a full white pattern in primary mode, and set-up 9300 degrees kelvin of picture white balance get the x,y value is x=0.281±0.01 y=0.311±0.01.

4.6. Screen Brightness Adjustment

1. Input a raster pattern in primary mode. Set external brightness key to recall value 50%, then make sure that the raster brightness range is 0.08FL.
2. Input a 2" pattern (video off) in primary mode. Set external contrast key to maximum and check that brightness at the center of the screen is in the range 41FL±1.
3. Input a full white pattern in primary mode. Set external brightness to 0.08FL. Adjust VR106 and check that brightness at the center of the screen is in the range 30FL±1.

Conclusion White Balance Adjustment:

4.7. Magnetic Field Configuration

Configure the magnetic field as follows:

- ☐ Northern hemisphere : H=0.01, V=0.45
- ☐ Southern hemisphere : H=0.01, V=-0.52

4.8. Raster Center Verification

Input a cross hatch pattern in 93.75kHz (1600x1200) mode, and check raster H-Center shall be less than 3mm (|L-R|≤3mm). If not in this ranged and select SW301 for adjustment raster H-center shall be less than 3mm, if not in this ranged again, please select SW302 for adjustment raster H-center in the specification.

4.9. Tilt Verification

Input a cross hatch pattern in primary mode and use the tilt rotation key to ensure that tilt is less than 1mm.

4.10. Focus Verification

1. Input a full white pattern in primary mode. Use the external brightness control to adjust background brightness so it is not visible and set external contrast so the brightness is 28FL, then switch to a display of cross hatch pattern.
2. Adjust the FBT focus VR1 and VR2 so the vertical line and horizontal line are as clear as possible.

4.11. Color Misconvergence

1. Switch to a cross hatch pattern select OSD menu to "Convergence" to value 50, adjust VR401, VR402 and verify that misconvergence in a circle measured from the center of the screen (Area A) is not greater than 0.3mm, and for all areas outside Area A is not greater than 0.4mm.
2. If not in the specification, after used the magnetic in a four corner adjustments for arrive to better color convergence.

Automatic camera alignment procedure:

The procedures listed below are those carried out using the automatic Camera Alignment System (CAS). These adjustments cannot be made manually but must be performed using the CAS software provided by the manufacturer.

4.12. Primary Test Mode Performance Adjustments

1. **V. RASTER CENTERING**
   Raster area centered vertically in the bezel.
2. **ROTATION (TILT)**
   Raster area aligned with bezel.

4.13. Performance Adjustments for All Preset Modes

1. **H POSITION**
   Centers the picture display horizontally in the bezel area (|L-R|≤3mm).
2. **H SIZE**
   Configures picture display width as 380± 3.0mm
3. **V POSITION**
   Centers the picture display vertically in the bezel area (|T-B|≤3mm).
4. **V SIZE**
   Configures picture display height as 285±3mm.
5. **Rotation**
   Configures picture display rotation as less than 3mm.
6. **Pin-Balance**
   Sets left and right pin-balance distortion to less than 2.0mm.
7. **PINCUSHION**
   Sets left and right pincushion distortion to less than 2.0mm.
8. **Trapezium**
   Sets upper and lower trapezium distortion to less than 2.0mm.

Conclusion of automatic alignment:

4.14. Image Performance Verification

Input each of the preset timings and check that the following specifications are met:

1. **Horizontal Position**
   |L-R|≤3.0mm
2. **Horizontal Size**
   380±3.0mm
3. **Vertical Position**
   |T-B|≤3.0mm
4. **Vertical Size**
   285±3mm
5. **Horizontal Linearity**
   VGA mode and full size:
   $$\left|\frac{MAX-AVG}{AVG}\right|<7\%$$
   Other modes :
   $$\left|\frac{MAX-AVG}{AVG}\right|<5\%$$
6. **Vertical Linearity**
   VGA mode and full size:
   $$\left|\frac{MAX-AVG}{AVG}\right|<7\%$$
   Other modes :
   $$\left|\frac{MAX-AVG}{AVG}\right|<5\%$$
7. **Recall Button Function**
   Adjust H/V phase and size at random using the external controls and press the recall button. Check that the image performance has returned to be in spec, which will indicate the recall button is functioning correctly.

4.15. Uniformity Verification

Input a full white pattern in primary mode, set contrast to maximum and check that there is no overshoot. Check that the brightness in the four corners of the screen is not less than 75% of that in the center of the screen.

4.16. Brightness Verification

1. Input a raster pattern (no video pattern) in primary mode. Adjust external brightness to maximum and measure the center of raster brightness is between 0.5 to 2.5FL.
2. Input a raster pattern (no video pattern) in primary mode. Adjust external brightness to 0.08FL (cut off).
3. Input a full white pattern and adjust external contrast to maximum then check that brightness at the center of the screen shall be more than 33±2FL.

4.17. Display Size Stability

Inputer a full white pattern in primary mode, set external brightness at 5FL and measure the display size. Adjust the brightness to 28FL and remeasure the display size. The difference should be less than 0.8mm.

4.18. Color Purity Verification

1. Input a full white pattern in primary mode and adjust external brightness so there is no background brightness and adjust external contrast to 25FL. Make a visual check of color purity as follows:
   a) Input the red (R) signal only; no green (G) or blue (B) should be visible.
   b) Input the (G) signal only; no (R) or B should be visible.
   c) Input the (B) signal only; no (R) or (G) should be visible.

4.19. Video Noise

Input a cross hatch pattern or full white pattern in primary mode and make a visual check from a distance of 18 inches for any video noise or other on-screen interference.

4.20. Power Saving Check

1. Input cross hatch pattern in primary mode.
2. Turn OFF H-Sync signal, the power indicator LED have to change the emitting color from green to orange, then turn ON H-Sync signal again, the picture shall be visible.
3. Turn OFF V-Sync signal, the power indicator LED have to change the emitting color from green to orange, then turn ON V-Sync signal again, the picture shall be visible.
4. Turn OFF H/V-Sync signal, the power indicator LED have to change the emitting color from green to orange, then turn ON H/V-Sync signal again, the picture shall be visible.

4.21. DDC 1/2 Data Writing

Writing the DDC 1/2 data in EEROM.

4.21.1. Mode : RTH-1H21

128 BYTES OF EDID CODE:

	0	1	2	3	4	5	6	7	8	9
0	00	FF	FF	FF	FF	FF	FF	00	34	38
10	72	1F	39	30	00	00	32	07	01	00
20	0C	28	1E	CA	E8	00	B2	A0	57	49
30	9B	26	10	48	4F	24	43	00	31	4A
40	31	59	45	59	61	59	81	99	A9	4F
50	01	01	01	01	86	3D	00	C0	51	00
60	30	40	44	A0	13	00	7C	1D	11	00
70	00	1E	1A	4F	40	30	62	B0	32	40
80	40	C0	13	00	7C	1D	11	00	00	1E
90	F9	15	20	F8	30	58	1F	20	20	40
100	13	00	7C	1D	11	00	00	1E	D5	09
110	80	A0	20	90	31	10	10	60	C2	00
120	7C	1D	11	00	00	1C	00	E4		

(08-09)
ID manufacturer name = MAX

(10-11)
Product ID code (dec code) = 8050(1F72)

(12-15)
Serial number= 12345

(16)
Week of manufacturer = 50

(17)
Year of manufacturer = 1997

(10-17)
Complete serial number (bar code label)=108050975012345

(18)
EDID structure version number = 1

(19)
EDID structure revision number = 0

(20)
Video input definition = Separate Sync
Composite sync, Analog signal, 0.700Vpp/0.300Vpp

(21)
Maximum horizontal image size = 40 cm

(22)
Maximum vertical image size = 30 cm

(23)
Display gamma = 3.02

(24)
DPMs supported feature = Stand By
Supspend, Active off display type = RGB color diaplay,
Chroma info : Hitachi CRT

(25-34)

- ☐ Red_x= 0.625, Green_x= 0.285, Blue_x= 0.150, White_x= 0.281
- ☐ Red_y= 0.340, Green_y= 0.605, Blue_y= 0.065, White_y= 0.311

(35) Established timing I :

- ☐ 720 x 400 @ 70Hz (VGA, IBM) .... NO
- ☐ 720 x 400 @ 88Hz (XGA2, IBM) .... NO
- ☐ 640 x 480 @ 60Hz (VGA, IBM) .... YES
- ☐ 640 x 480 @ 67Hz (MAC II, APPLE) .... NO
- ☐ 640 x 480 @ 72Hz (VESA) .... NO
- ☐ 640 x 480 @ 75Hz (VESA) .... YES
- ☐ 800 x 600 @ 56Hz (VESA) .... NO
- ☐ 800 x 600 @ 60Hz (VESA) .... NO

(36) Established timing II :

- ☐ 800 x 600 @ 72Hz (VESA) .... NO
- ☐ 800 x 600 @ 75Hz (VESA) .... YES
- ☐ 832 x 624 @ 75Hz (MAC II , APPLE) .... NO
- ☐ 1024 x 768 @ 87Hz (interlace)(8514A, IBM) .. NO
- ☐ 1024 x 768 @ 60Hz (VESA) .... NO
- ☐ 1024 x 768 @ 70Hz (VESA) .... NO
- ☐ 1024 x 768 @ 75Hz (VESA) .... YES
- ☐ 1280 x 1024 @ 75Hz (VESA) .... YES

(37)
Manufacturer's reserved timing :

- ☐ 1152 x 870 @ 75Hz (MAC II , APPLE) .... NO

Manufacturer's timing (Support for VESA DDC V1.0p rev:1.6p):

- ☐ 640 x 480 @ 85Hz (VESA) .... NO
- ☐ 800 x 600 @ 85Hz (VESA) .... NO
- ☐ 1024 x 768 @ 85Hz (VESA) .... NO
- ☐ 1280 x 1024 @ 85Hz (VESA) .... NO
- ☐ 1600 x 1280 @ 75Hz (VESA) .... NO
- ☐ 1600 x 1200 @ 85Hz (VESA) .... NO
- ☐ EDID Ver 1, REV 0 FLAG .... NO

(38-53)
Standard Timing Identification:

- ☐ #1 : 640 x 400 @ 70Hz Image_Asp_Ratio= 4:3
- ☐ #2 : 640 x 480 @ 85Hz Image_Asp_Ratio= 4:3
- ☐ #3 : 800 x 600 @ 85Hz Image_Asp_Ratio= 4:3
- ☐ #4 : 1024 x 768 @ 85Hz Image_Asp_Ratio= 4:3
- ☐ #5 : 1280 x 1024 @ 85Hz Image_Asp_Ratio= 5:4
- ☐ #6 : 1600 x 1200 @ 75Hz Image_Asp_Ratio= 4:3
- ☐ #7 : (0x01h) Not Specified
- ☐ #8 : (0x01h) Not Specified

(54-71)
Detailed Timing Description:

- ☐ #1 :1280 x 1024
- ☐ Pixel Clock=157.50MHz
- ☐ Horizontal Image Size= 380mm
- ☐ Vertical Image Size= 285mm
- ☐ Refresh Mode :Non-interlace

Horizontal :

- ☐ Active Time=1280 pixels
- ☐ Blanking Time = 448 pixels
- ☐ Sync offset= 68 pixels
- ☐ Sync Pulse Width= 160 pixels
- ☐ Border= 0 pixels
- ☐ H-sync Frequency= 91.15 KHz

Vertical :

- ☐ Active Time=1024 lines
- ☐ Blanking Time = 48 lines
- ☐ Sync offset=1 lines
- ☐ Sync Pulse Width= 3 lines
- ☐ Border = 0 lines
- ☐ V-sync Frequency= 85.02Hz
- ☐ Sync configuration: Digital Separate, V-SYNC(+) , H-SYNC(+)

(72-89)
Detailed Timing Description:

- ☐ #2 : 1600 x 1200
- ☐ Pixel Clock=202.50MHz
- ☐ Horizontal Image Size= 380mm
- ☐ Vertical Image Size= 285mm
- ☐ Refresh Mode : Non-interlace

Horizontal :

- ☐ Active Time=1600 pixels
- ☐ Blanking Time = 560 pixels
- ☐ Sync offset= 64 pixels
- ☐ Sync Pulse Width= 192 pixels
- ☐ Border= 0 pixels
- ☐ H-sync Frequency= 93.75KHz

Vertical :

- ☐ Active Time=1200 lines
- ☐ Blanking Time = 50 lines
- ☐ Sync offset= 1 lines
- ☐ Sync Pulse Width= 3 lines
- ☐ Border= 0 lines
- ☐ V-sync Frequency= 75.00Hz

- ☐ Sync configuration: Digital Separate, V-SYNC(+) , H-SYNC(+)

(90-107)
Detailed Timing Description:

- ☐ #3 : 800 x 600
- ☐ Pixel Clock=56.25MHz
- ☐ Horizontal Image Size= 380mm
- ☐ Vertical Image Size= 285mm
- ☐ Refresh Mode : Non-interlace

Horizontal :

- ☐ Active Time= 800 pixels
- ☐ Blanking Time = 248 pixels
- ☐ Sync offset= 32 pixels
- ☐ Sync Pulse Width= 64 pixels
- ☐ Border= 0 pixels
- ☐ H-sync Frequency= 53.67KHz

Vertical :

- ☐ Active Time= 600 lines
- ☐ Blanking Time = 31 lines
- ☐ Sync offset= 1 lines
- ☐ Sync Pulse Width= 3 lines
- ☐ Border= 0 lines
- ☐ V-sync Frequency= 85.06Hz
- ☐ Sync configuration : Digital Separate, V-SYNC(+) , H-SYNC(+)

(108-125)
Detailed Timing Description:

- ☐ #4 : 640 x 400
- ☐ Pixel Clock=25.17MHz
- ☐ Horizontal Image Size= 380mm
- ☐ Vertical Image Size= 285mm
- ☐ Refresh Mode : Non-interlace

Horizontal :

- ☐ Active Time= 640 pixels
- ☐ Blanking Time = 160 pixels
- ☐ Sync offset= 16 pixels
- ☐ Sync Pulse Width= 96 pixels
- ☐ Border= 0 pixels
- ☐ H-sync Frequency= 31.46 KHz

Vertical :

- ☐ Active Time= 400 lines
- ☐ Blanking Time = 49 lines
- ☐ Sync offset= 12 lines
- ☐ Sync Pulse Width= 2 lines
- ☐ Border= 0 lines
- ☐ V-sync Frequency= 70.07 Hz
- ☐ Sync configuration: Digital Separate, V-SYNC(+) , H-SYNC(-)

- ☐ EDID Checksum byte = (0xE4)............. OK

4.21.2. Mode : RTH-1H21

128 BYTES OF EDID CODE :

	0	1	2	3	4	5	6	7	8	9
0	00	FF	FF	FF	FF	FF	FF	00	40	A1
10	8F	05	39	30	00	00	0D	08	01	00
20	0E	28	1E	CA	E8	00	B2	A0	57	49
30	9B	26	10	48	4F	24	43	00	31	4A
40	31	59	45	59	61	59	81	99	A9	4F
50	01	01	01	01	86	3D	00	C0	51	00
60	30	40	44	A0	13	00	7C	1D	11	00
70	00	1E	1A	4F	40	30	62	B0	32	40
80	40	C0	13	00	7C	1D	11	00	00	1E
90	F9	15	20	F8	30	58	1F	20	20	40
100	13	00	7C	1D	11	00	00	1E	D5	09
110	80	A0	20	90	31	10	10	60	C2	00
120	7C	1D	11	00	00	1C	00	8E		

(08-09)
ID Manufacturer Name = PEA

(10-11)
Product ID Code (Dec Code) = 1423(58F)

(12-15)
Serial Number = 12345

(16)
Week Of Manufacturer = 13

(17)
Year Of Manufacturer = 1998

(10-17)
Complete serial number(bar code label)=50121423981312345

(18)
EDID Structure Version Number = 1

(19)
EDID Structure Revision Number = 0

(20)
VIDEO INPUT DEFINITION = Separate Sync, Composite Sync, Sync on Green, Analog Signal, 0.700Vpp/0.300Vpp

(21)
Maximum Horizontal Image Size = 40cm

(22)
Maximum Vertical Image Size = 30cm

(23)
Display Gamma = 3.02

(24)
DPMS Supported Feature= Stand By
Supspend, Active off Display Type = RGB color diaplay
Chroma info : Hitachi CRT

(25-34)

- Red_x= 0.625 Green_x= 0.285 Blue_x= 0.150 White_x= 0.281
- Red_y= 0.340 Green_y= 0.605 Blue_y= 0.065 White_y= 0.311

(35)
Established timing I :

- 720 x 400 @ 70Hz (VGA ,IBM) .... NO
- 720 x 400 @ 88Hz (XGA2,IBM) .... NO
- 640 x 480 @ 60Hz (VGA ,IBM) .... YES
- 640 x 480 @ 67Hz (MAC II ,APPLE) .... NO
- 640 x 480 @ 72Hz (VESA) .... NO
- 640 x 480 @ 75Hz (VESA) .... YES
- 800 x 600 @ 56Hz (VESA) .... NO
- 800 x 600 @ 60Hz (VESA) .... NO

(36)
Established timing II :

- 800 x 600 @ 72Hz (VESA) .... NO
- 800 x 600 @ 75Hz (VESA) .... YES
- 832 x 624 @ 75Hz (MAC II ,APPLE) .... NO
- 1024 x 768 @ 87Hz (interlace) (8514A, IBM). . NO
- 1024 x 768 @ 60Hz (VESA) .... NO
- 1024 x 768 @ 70Hz (VESA) .... NO
- 1024 x 768 @ 75Hz (VESA) .... YES
- 1280 x 1024 @ 75Hz (VESA) .... YES

(37)
Manufacturer's reserved timing :

- 1152 x 870 @ 75Hz (MAC II, APPLE) .... NO

Manufacturer's timing (Support for VESA DDC V1.0p rev:1.6p) :

- 640 x 480 @ 85Hz (VESA) .... NO
- 800 x 600 @ 85Hz (VESA) .... NO
- 1024 x 768 @ 85Hz (VESA) .... NO
- 1280 x 1024 @ 85Hz (VESA) .... NO
- 1600 x 1280 @ 75Hz (VESA) .... NO
- 1600 x 1200 @ 85Hz (VESA) .... NO
- EDID Ver 1, REV 0 FLAG................. NO

(38-53)
Standard Timing Identification :

- #1: 640 x 400 @ 70Hz Image_Asp_Ratio= 4:3
- #2: 640 x 480 @ 85Hz Image_Asp_Ratio= 4:3
- #3: 800 x 600 @ 85Hz Image_Asp_Ratio= 4:3
- #4: 1024 x 768 @ 85Hz Image_Asp_Ratio= 4:3
- #5: 1280 x 1024 @ 85Hz Image_Asp_Ratio= 5:4
- #6: 1600 x 1200 @ 75Hz Image_Asp_Ratio= 4:3
- #7: (0x01h) Not Specified
- #8: (0x01h) Not Specified

(54-71)
Detailed Timing Description :

- #1 : 1280 x 1024
- Pixel Clock=157.50MHz
- Horizontal Image Size= 380mm
- Vertical Image Size= 285mm
- Refresh Mode : Non-interlace

Horizontal :

- Active Time=1280 pixels
- Blanking Time = 448 pixels
- Sync offset= 68 pixels
- Sync Pulse Width= 160 pixels
- Border= 0 pixels
- H-sync Frequency= 91.15KHz

Vertical :

- Active Time=1024 lines
- Blanking Time = 48 lines
- Sync offset= 1 lines
- Sync Pulse Width= 3 lines
- Border= 0 lines
- V-sync Frequency= 85.02Hz
- Sync configuration : Digital Separate, V-SYNC(+) , H-SYNC(+)

(72-89)
Detailed Timing Description :

- #2 : 1600 x 1200
- Pixel Clock=202.50MHz
- Horizontal Image Size= 380mm
- Vertical Image Size= 285mm
- Refresh Mode : Non-interlace

Horizontal :

- Active Time=1600 pixels
- Blanking Time = 560 pixels
- Sync offset= 64 pixels
- Sync Pulse Width= 192 pixels
- Border= 0 pixels
- H-sync Frequency= 93.75KHz

Vertical :

- Active Time=1200 lines
- Blanking Time = 50 lines
- Sync offset= 1 lines
- Sync Pulse Width= 3 lines
- Border= 0 lines
- V-sync Frequency= 75.00Hz
- Sync configuration : Digital Separate, V-SYNC(+) , H-SYNC(+)

(90-107)
Detailed Timing Description :

- #3 : 800 x 600
- Pixel Clock=56.25MHz
- Horizontal Image Size= 380mm
- Vertical Image Size= 285mm
- Refresh Mode :Non-interlace

Horizontal :

- Active Time= 800 pixels
- Blanking Time = 248 pixels
- Sync offset= 32 pixels
- Sync Pulse Width= 64 pixels
- Border= 0 pixels
- H-sync Frequency= 53.67kHz

Vertical :

- Active Time= 600 lines
- Blanking Time = 31 lines
- Sync offset= 1 lines
- Sync Pulse Width= 3 lines
- Border= 0 lines
- V-sync Frequency= 85.06Hz
- Sync configuration : Digital Separate, V-SYNC(+) , H-SYNC(+)

(108-125)
Detailed Timing Description :

- #4 : 640 x 400
- Pixel Clock=25.17MHz
- Horizontal Image Size= 380mm
- Vertical Image Size= 285mm
- Refresh Mode : Non-interlace

Horizontal :

- Active Time= 640 pixels
- Blanking Time = 160 pixels
- Sync offset=16 pixels
- Sync Pulse Width= 96 pixels
- Border= 0 pixels
- H-sync Frequency= 31.46 KHz

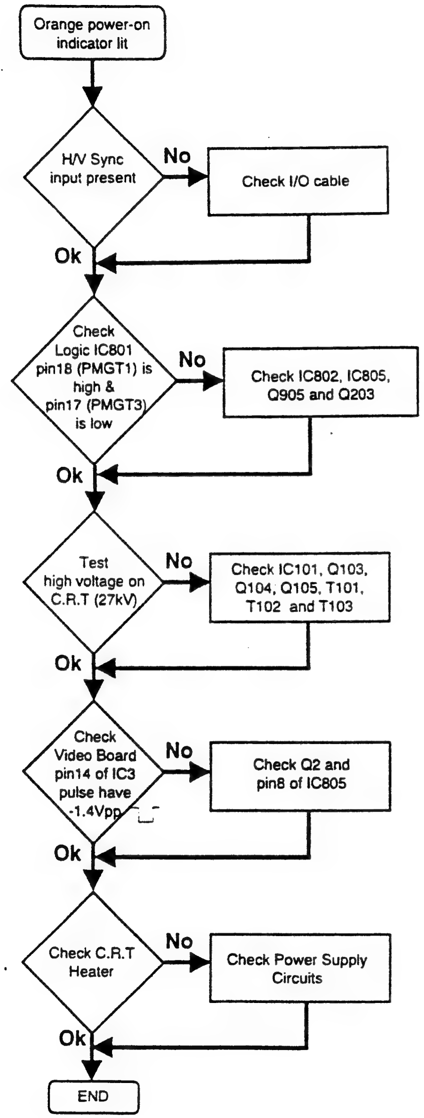
Vertical :

- Active Time= 400 lines
- Blanking Time = 49 lines
- Sync offset= 12 lines
- Sync Pulse Width= 2 lines
- Border= 0 lines
- V-sync Frequency= 70.07Hz
- Sync configuration : Digital Separate, V-SYNC(+) , H-SYNC(-)
- EDID Checksum byte (0x8E) .... OK

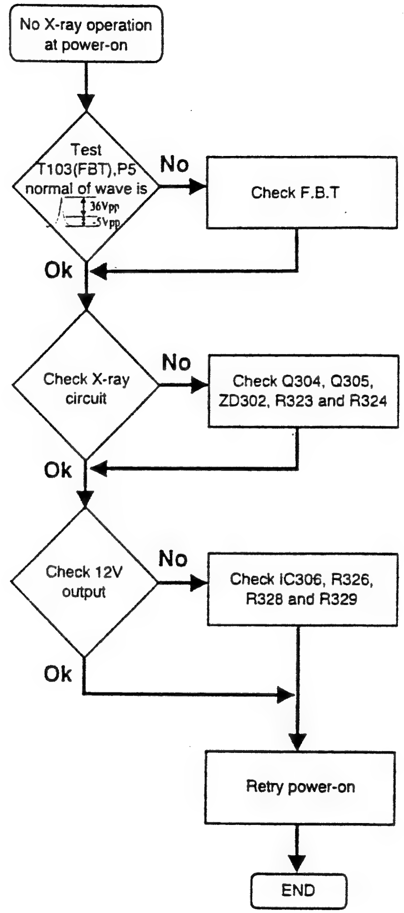
Notes

Section 5.
Troubleshooting

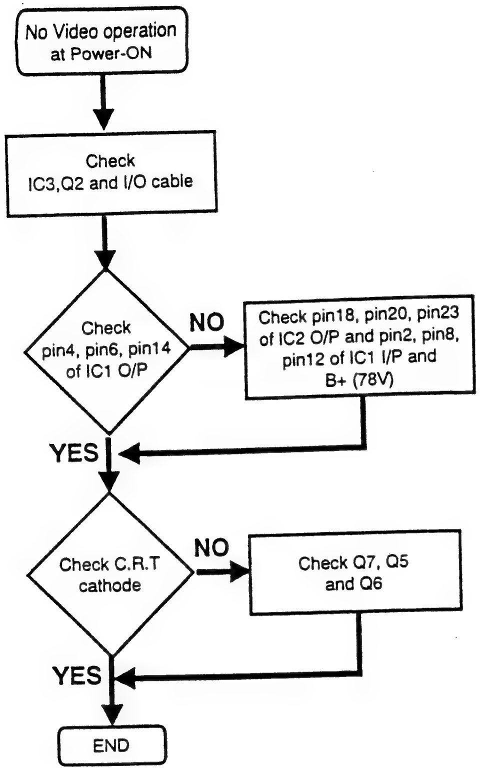
5.1. No Display at Power-on



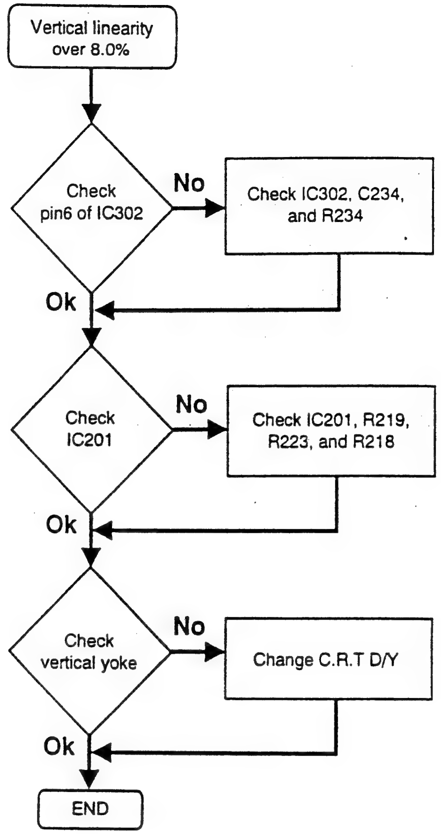
5.2. No X-ray Operation



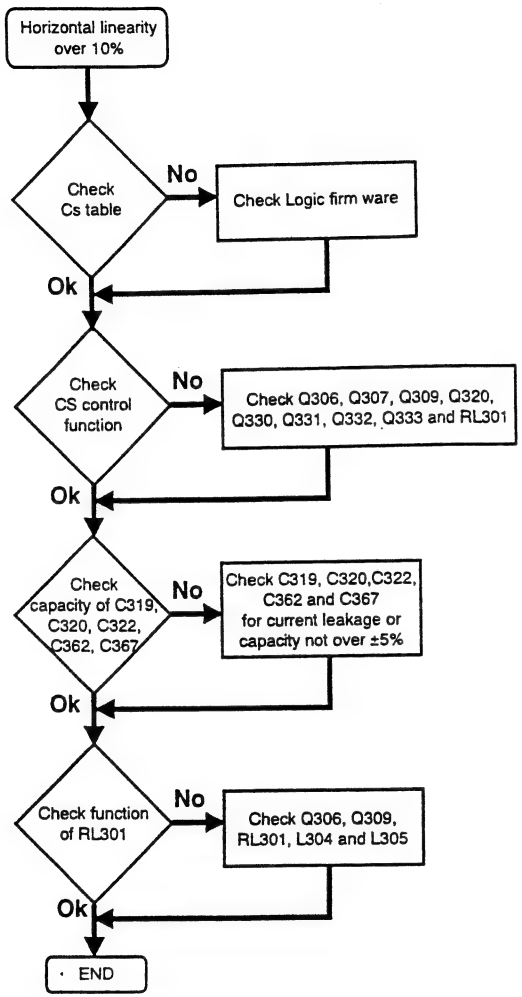
5.3. No Video Operation



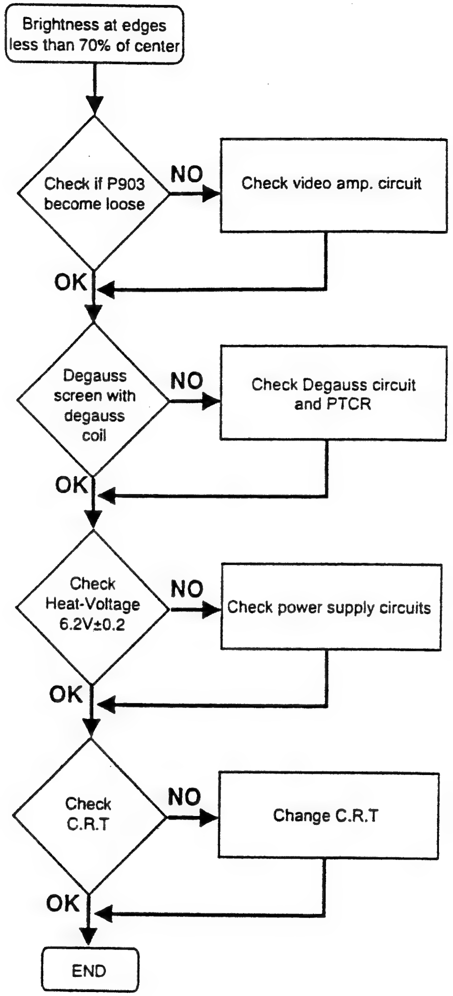
5.4. Poor Vertical Linearity



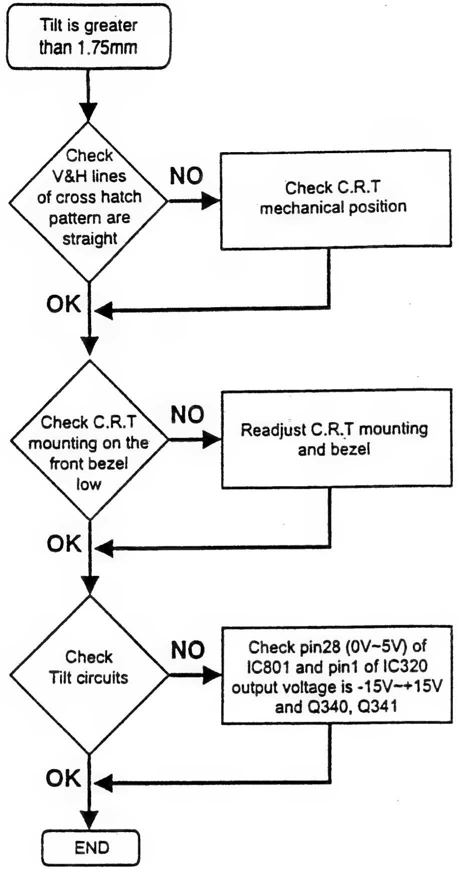
5.5. Poor Horizontal Linearity



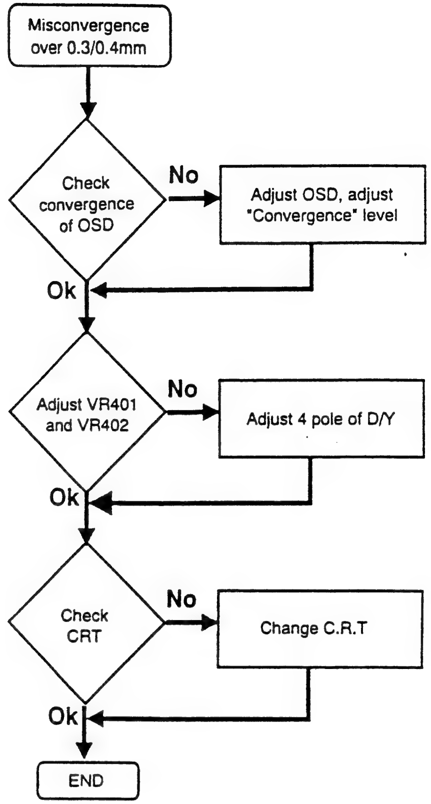
5.6. Poor Uniformity



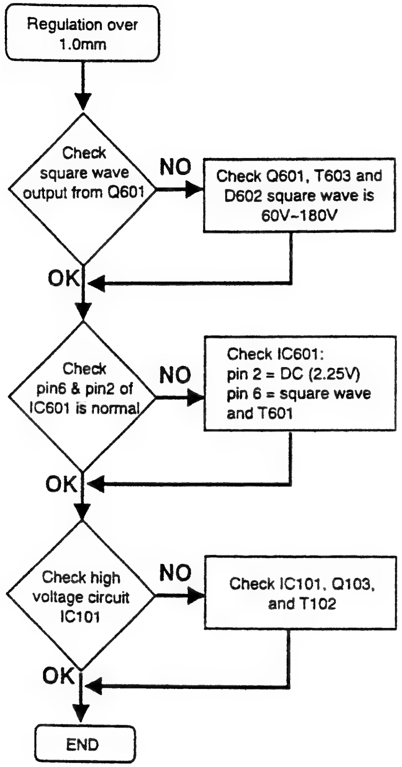
5.7. Tilted Display Area



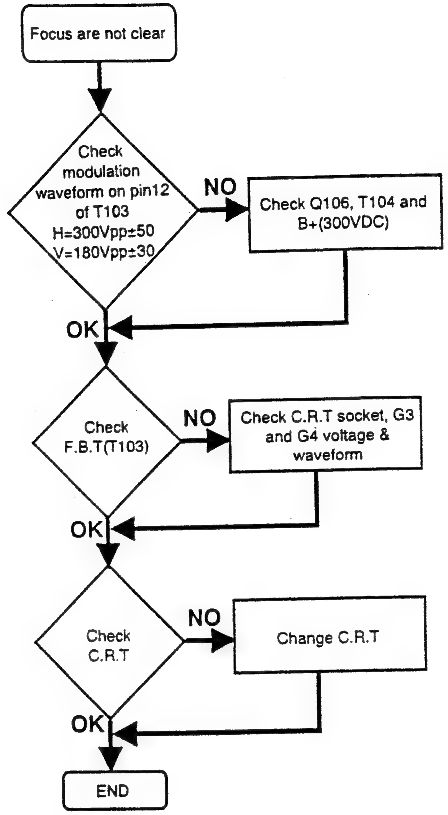
5.8. Misconvergence



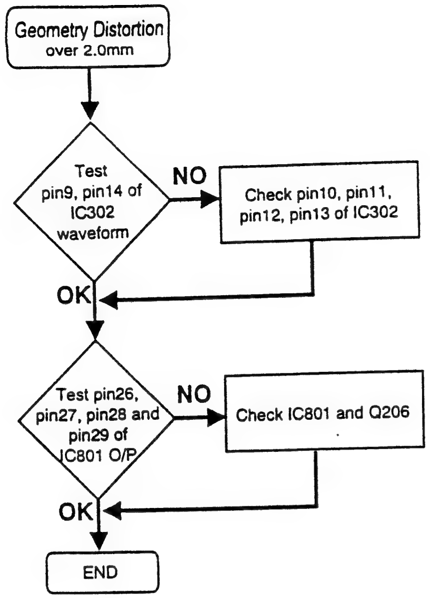
5.9. Poor Regulation



5.10. Poor Focus



5.11. Poor Geometry Distortion



Section 6. Printed Circuit Boards

6.1. Neck Board

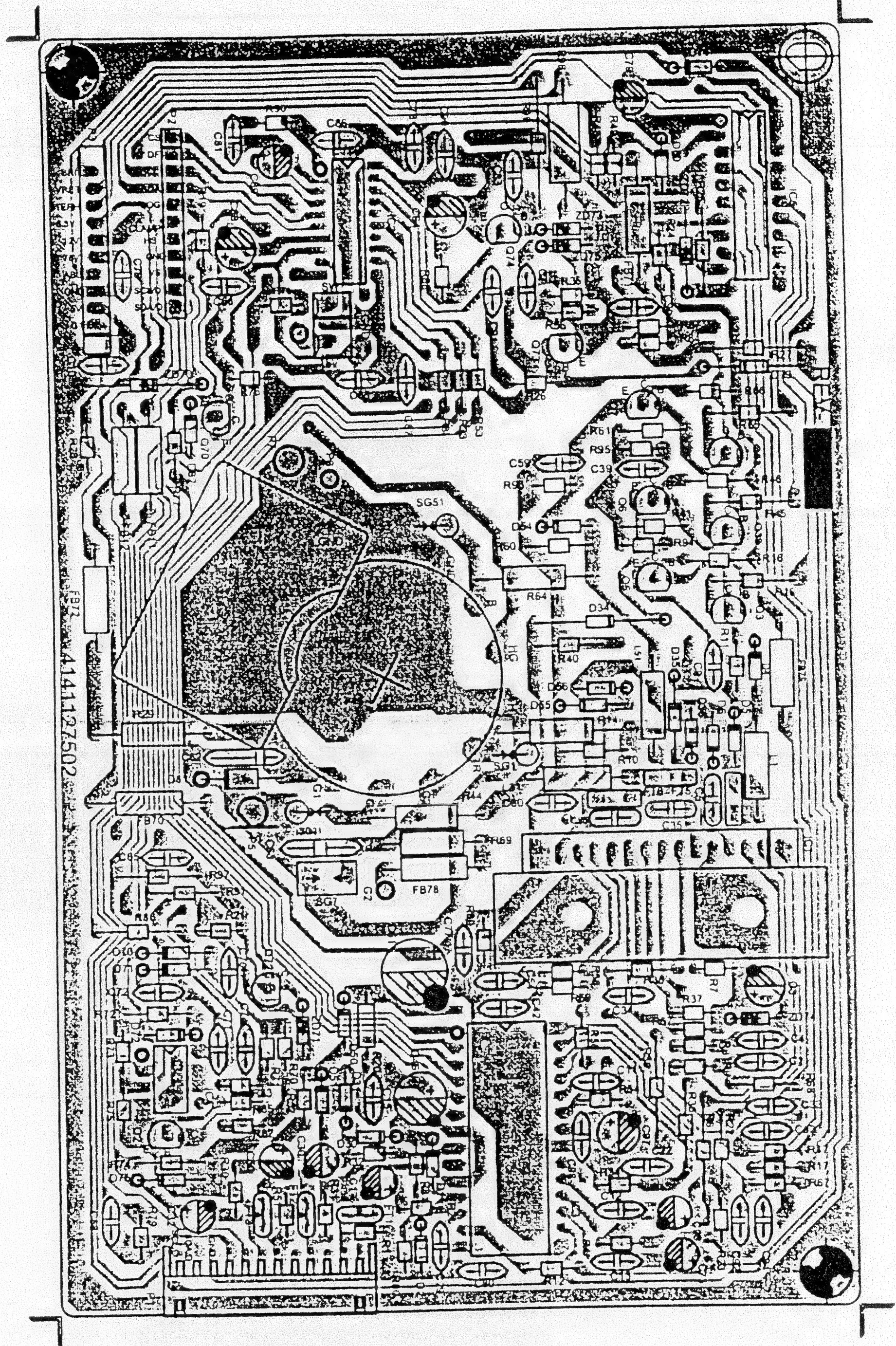


Figure 6-1 Neck Board (Solder Side)

6.2. Control Board

6.2.1. Model NO. : RTH-1H21

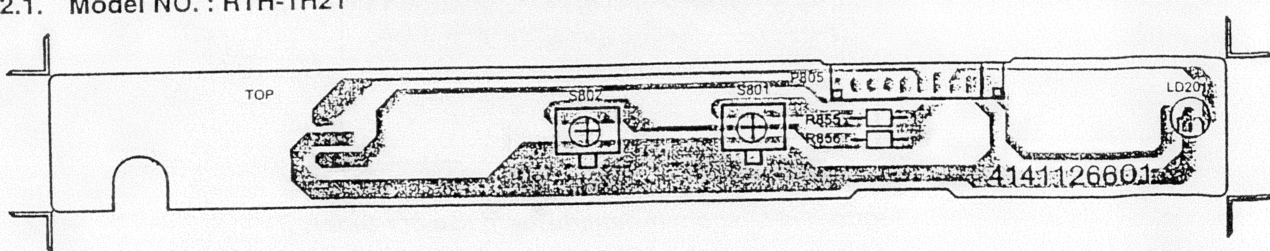


Figure 6-2 Control Board (Solder Side)

6.2.2. Model NO. : RTH-1H26

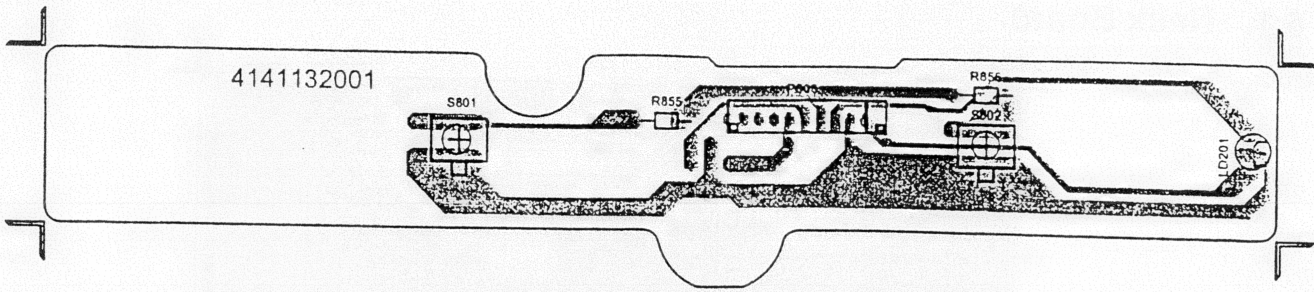
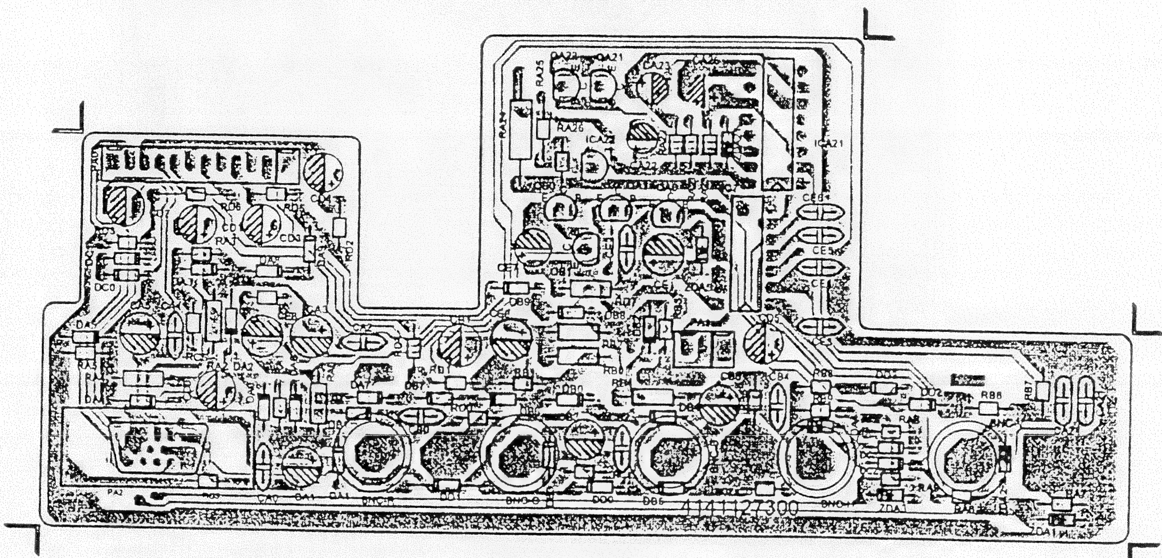


Figure 6-3 Control Board (Solder Side)

6.3. Video Switch Board



6-4 Video Switch Board (Solder Side)

6.4. Misconvergence Board

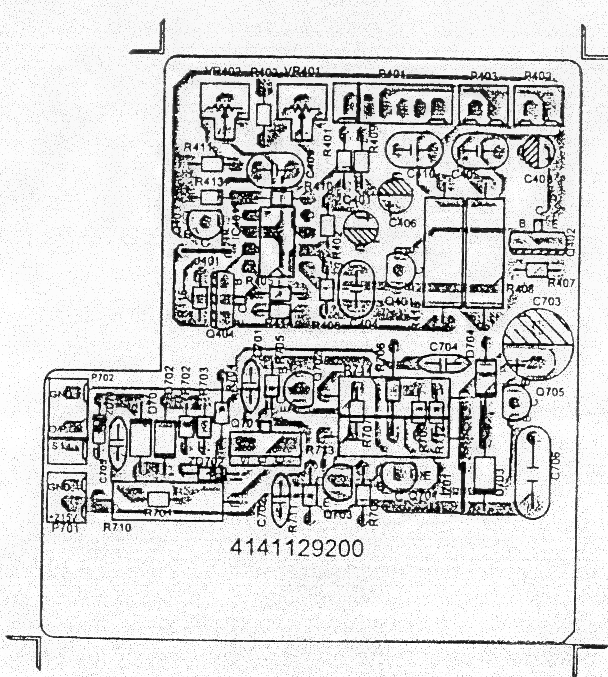


Figure 6-5 Misconvergence Board (Solder Side)

6.5. Main Board

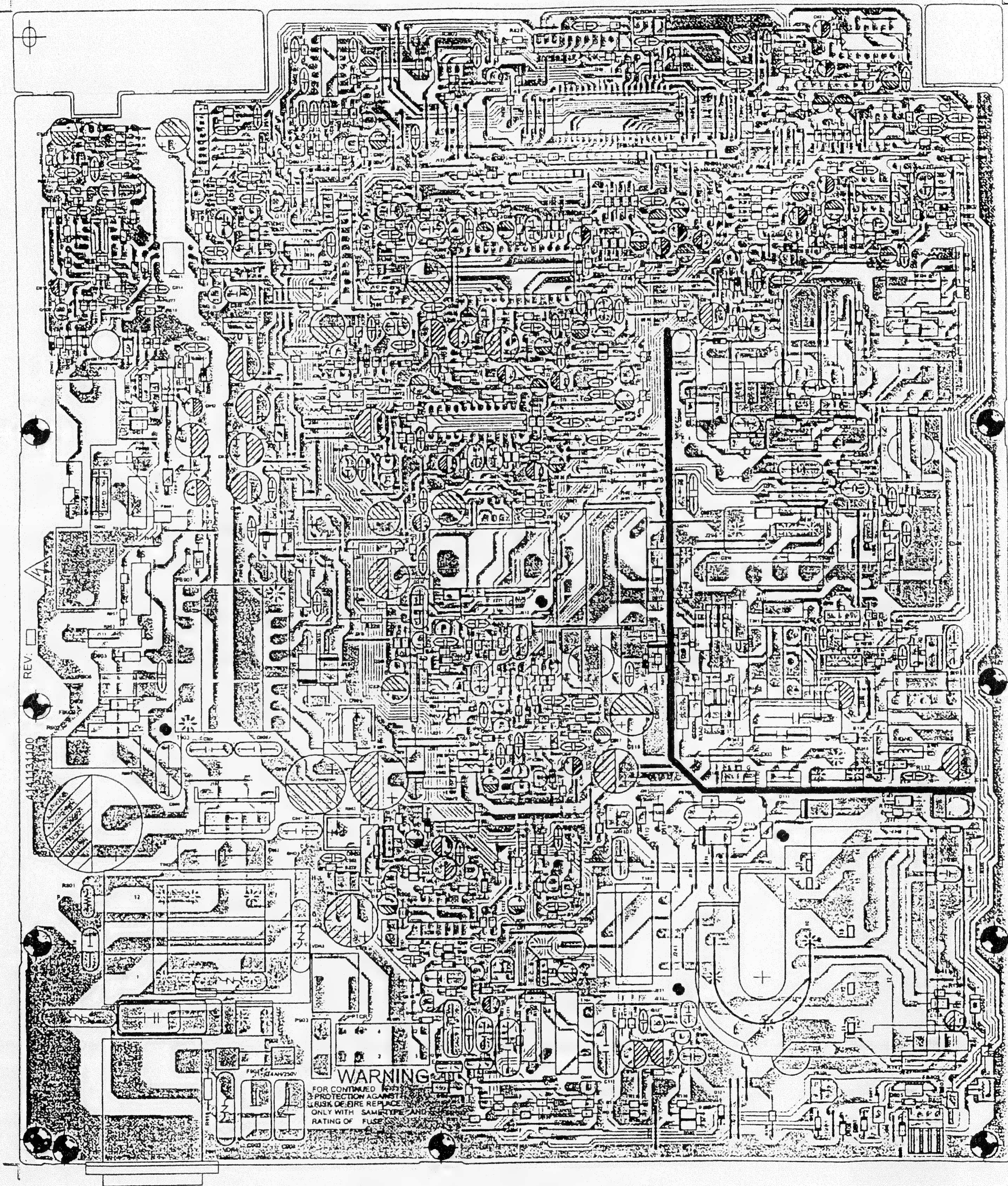


Figure 6-6 Main Board (Solder Side)

6.6. PCB Wiring Connection

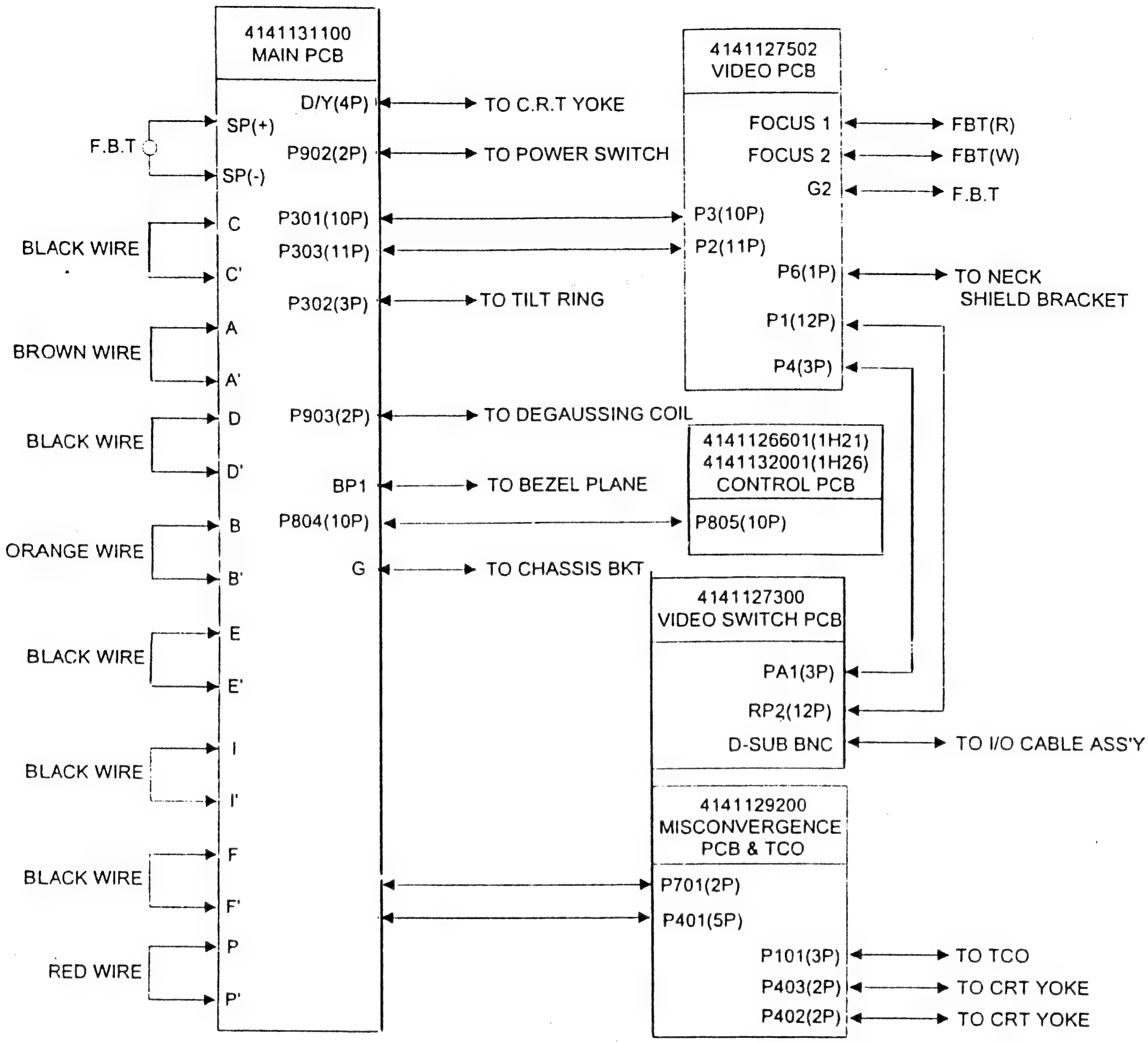


Figure 6-7 PCB Wiring Connection

Section 7.

Schematic Diagrams

7.1. Neck Circuit Diagram

Please refer to the attached circuit diagram.

7.2. BNC Circuit Diagram

Please refer to the attached circuit diagram.

7.3. SPS and Deflection Circuit Diagram

Please refer to the attached circuit diagram.

Section 8.

Mechanical Parts

8.1. Key to Exploded View

REF.	PART NO.	DESCRIPTION
1	8127113008	SCREW PAN(+)/HD CAP M3X8 TAPPI FOR BEZEL & U-BKT
2	1S010R1H21	#BEZEL FOR RTH-1H21
	1S01091H26	#BEZEL FOR RTH-1H26
3	2018091H20	AEF PLATE FOR BEZEL
	C4607F4120	WIRE ASS'Y 300MM FOR BEZEL MATEL
4	8418113015	SCREW BID(+) TAPPING M3X15 ZIN FOR CONTROL PANEL & BEZEL X3
5	5550650187	COPPER TAPE #65mm FOR CRT
6	1SA70G7D20	POWER KNOB
7	2011097H10	POWER SPRING
8	1S210R1H20	#CONTROL PANEL FOR RTH-1H21
	1S21091H23	#CONTROL PANEL FOR RTH-1H26
9	1SA60R7H10	ROTARY KNOB FOR RTH-1H21
	1SA70G7K40	ROTARY KNOB FOR RTH-1H26
10	8081111530	SCREW BIND/HD MACH 1/4"-20X30 FOR BASE & RETAINER
11	1SAM0R7H10	PIANO KEY B FOR RTH-1H21
	1SAM091H23	PIANO KEY FOR RTH-1H26
12	TH1H200444-V	CONTROL PCB ASS'Y FOR RTH-1H21
	TH1H230444-V	CONTROL PCB ASS'Y FOR RTH-1H26
13	4410202006	POWER SWITCH SS-160-7D SPST FOR SW901
14	8418113010	SCREW BIND(+) TAPPING M3X10 ZI FOR CONT. PANEL & PCB X3, CONT. PANEL & PW SW X2
15	4410516330	TCO MYLAR W/CARBON FOR YOKE
16	7010035621	#CRT M51LCJ183X95 (FMU) FOR HITACHI CRT
17	C001131H20	CRT BRAID WIRE ASS'Y
18	2004091H20	#CRT FRAME
19	C371H20010	WASHER ASS'Y FOR CRT FRAME & BEZEL
20	8418115025	SCREW BID(+)/HD TAPPING M5X25 FOR BEZEL & CRT FRAME
21	7020211H20	DEGAUSSING COIL
22	TH1H210144-V	MAIN PCB ASS'Y
23	3011100030	NUT ISO HEX M3 Z1NC FOR AC LINE FILTER X2, TCO & MISCON.PCB FIX
24	8127113006	SCREW PAN(+)/HD CAP TAPPING M3 TOP SHIELD & U-BKT X4,CRT FRAME & TOP SHIELD X2, CRT FRAME & U BKT X2,U-BKT & U-BKT HOLDER X4, U-BKT & MAIN PCB X5
25	8026113006	SCREW B/HD M3X6 TAPPING "B" FOR BTM SHIELD & U-BKT, U-BKT & MAIN PCB X2
26	TH1H200644-V	MISCONVERGENCE PCB ASS'Y FOR RTH-1H21
	TH1H260644-V	MISCONVERGENCE PCB ASS'Y FOR RTH-1H26
27	8504113008	SCREW BIND(+) M3X8 MACH W/DISK FOR TCO & MISCON.PCB FIX X2,U-BKT & BNC STUD X3
28	36523LSC12	SPACER SUPPORT (LSC-12) FOR BOTTOM SHIELD
29	2001192H24	#BOTTOM SHIELD
30	2001192H20	U-BKT HOLDER
31	TH1H200544-V	VIDEO SWITCH PCB ASS'Y
32	2008092H20	#STUD M3X12 FOR BNC PCB
33	2007092H20	BNC SHIELD
34	2001091H20	U BRACKET
35	9005091H21	#DECO PLATE (BNC)
36	C7101H2120	I/O CABLE D-SUB TO BNC 6FT ASS'Y FOR RTH-1H21
	C7101H2610	I/O CABLE D-SUB TO BNC 6FT ASS'Y FOR RTH-1H26
37	7067F20122	LINE FILTER IX-0342-P FOR P901
38	8504113010	SCREW BIND(+) M3X10 MACH W/DISK FOR FILTER & U-BKT X2
39	8026153008	SCREW B/HD M3X8 TAPPING "B" FOR VIDEO COVER & IC1 HEAT SINK ASS'Y
40	2006099H10	NECK COVER (F)
41	2007099H10	NECK SHIELD
42	TH1H200244-V	NECK PCB ASS'Y
43	2008097H10	NECK COVER (B)
44	9010091H20	#UL SPONGE 80X70X60
45	2002191H20	#TOP SHIELD
46	2003092H20	REAR SHIELD
47	1S020R2H20	#BUCKET FOR RTH-1H21
	1S02092H20	#BUCKET FOR RTH-1H26
48	8059114045	SCREW BIND(+) B-2 M4X45 TAPPIN FOR BEZEL & BUCKET
49	1006194251	#RETAINER
50	1S040R2H20	#TILT BALL FOR RTH-1H21
	1S04092H20	#TILT BALL FOR RTH-1H26
51	1S050R2H20	#BASE FOR RTH-1H21
	1S05092H20	#BASE FOR RTH-1H26
52	1019194230	FOOT
53	8026113015	SCREW STEEL TRI "B" TAPPING BI FOR U-BKT HOLDER & TILT BALL

Other parts list

REF.	PART NO.	DESCRIPTION
	1023094330	SPACER RING FOR FBT
	1026094000	MOVABLE BUSHING FOR CRT FRAME
	2004197H10	HEAT SINK FOR VIDEO COVER & IC1 HEAT SINK ASS'Y
	3011100040	NUT M4 ZN3C FOR NECK SCREW & GND WIRE FIX
	367232A007	WIRE LOCK FOR FBT WIRE
	36823FW003	WIRE MOUNTS FOR CRT FRAME FOR RTH-1H21
	36823FW003	WIRE MOUNTS FOR CRT FRAME FOR RTH-1H26
	36823TA103	WIRE HOLDER TA10-35 FOR FBT COVER & DY WIRE X1
	36823TA103	WIRE HOLDER TA10-35 FOR TOP SHIELD
	4141129100	P.C.B. SENSOR BAR FOR CRT
	4490100204	CONN. BNC 180 DEGREE FOR R,G,B,H,V
	463160000N	AC POWER CORD WALL VDE 6FT GE#
	5290005000	TUBE-SHRINK ID=5¢ FOR SW901
	5530200102	CORD CRAMPER TH-A FOR NECK SHIELD (F)
	5541025095	CABLE TIE 2.5X90 FOR DEGAUSSING COIL X9,TCO WIRE X1
	5541036300	CABLE TIE 3.6X300MM. FOR DEGAUSSING COIL
	555019S001	CLOTH FILM TAPE #19mm
	555040S002	CLOTH FILM TAPE #40mm FOR AEF PLATE
	555040S002	CLOTH FILM TAPE #40mm FOR SENSOR BAR FIX
	555160S143	#ADHESIVE FOR SENSOR BAR
	8026113006	SCREW B/HD M3X6 TAPPING "B" FOR PCB & Q902 HEAT SINK X2
	9006092H20	CRT CUSION
	9012A91H21	MANUAL & TCO ASS'Y

REF	PART NO.	DESCRIPTION
	9018095L41	WARRANTY STICKER
	C4595G1112	GND WIRE ASS'Y FOR U-BKT TO VIDEO SHIELD
	C4597A1010	GND WIRE ASS'Y 70mm FOR VIDEO SHIELD TO NECK SCREW
	C4597F1012	GND WIRE ASS'Y FOR VIDEO SHIELD TO U-BRACKET
	C488020183	CONN. 2P & WIRE ASS'Y FOR SENSOR BAR
	C488031217	CONN. 3P & WIRE ASS'Y 400mm FOR P902

8.2. Exploded View

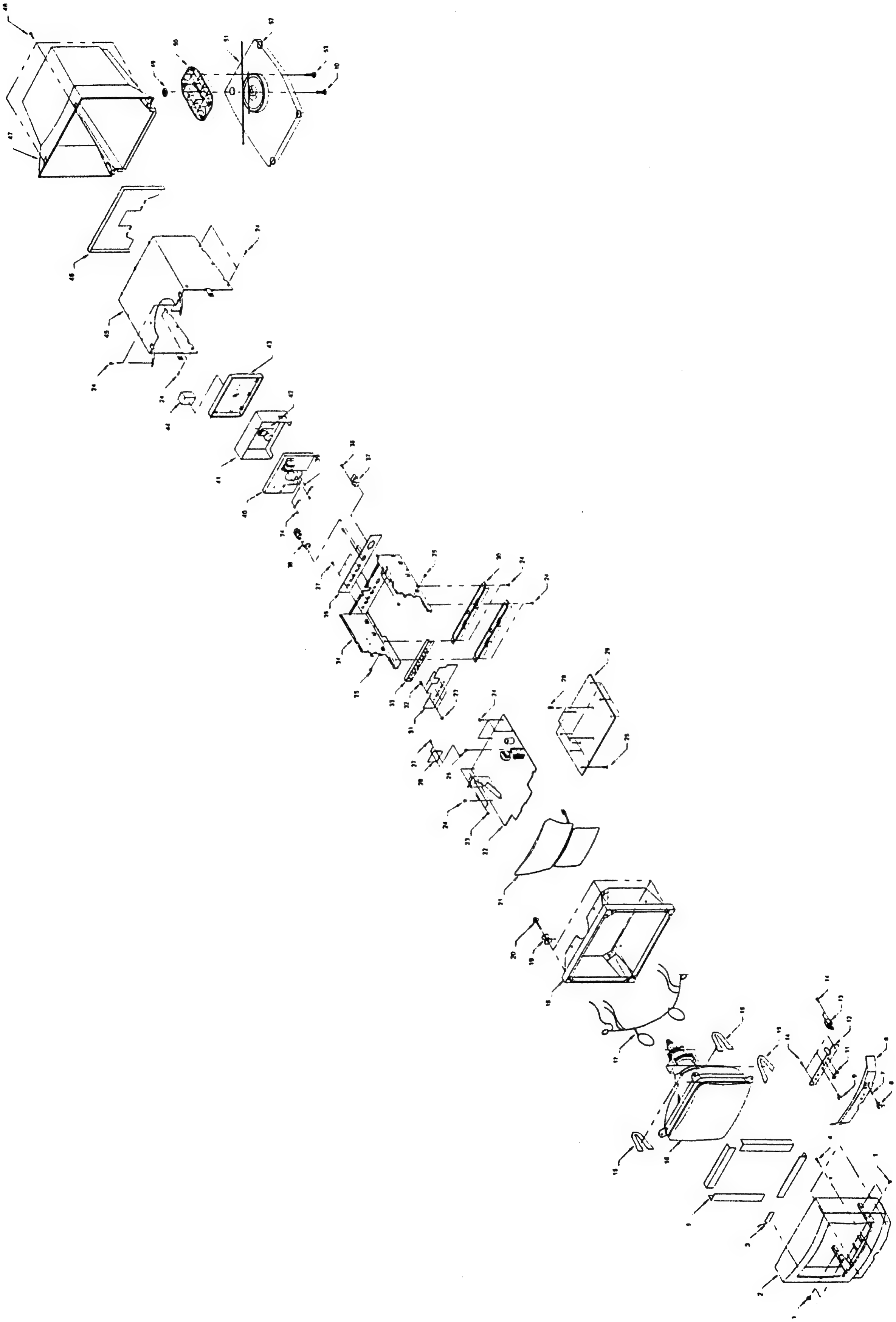
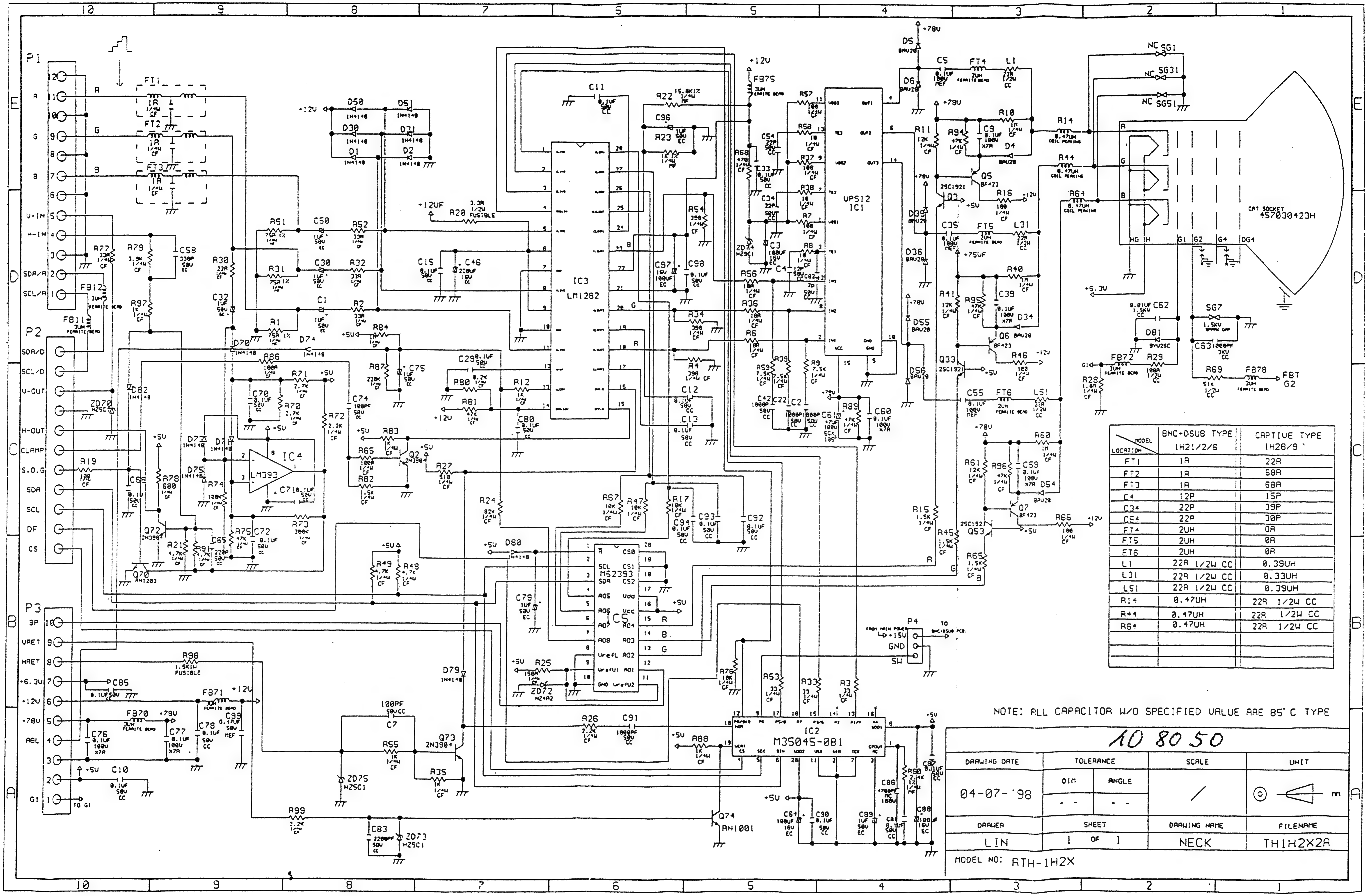


Figure 8-1 Exploded View



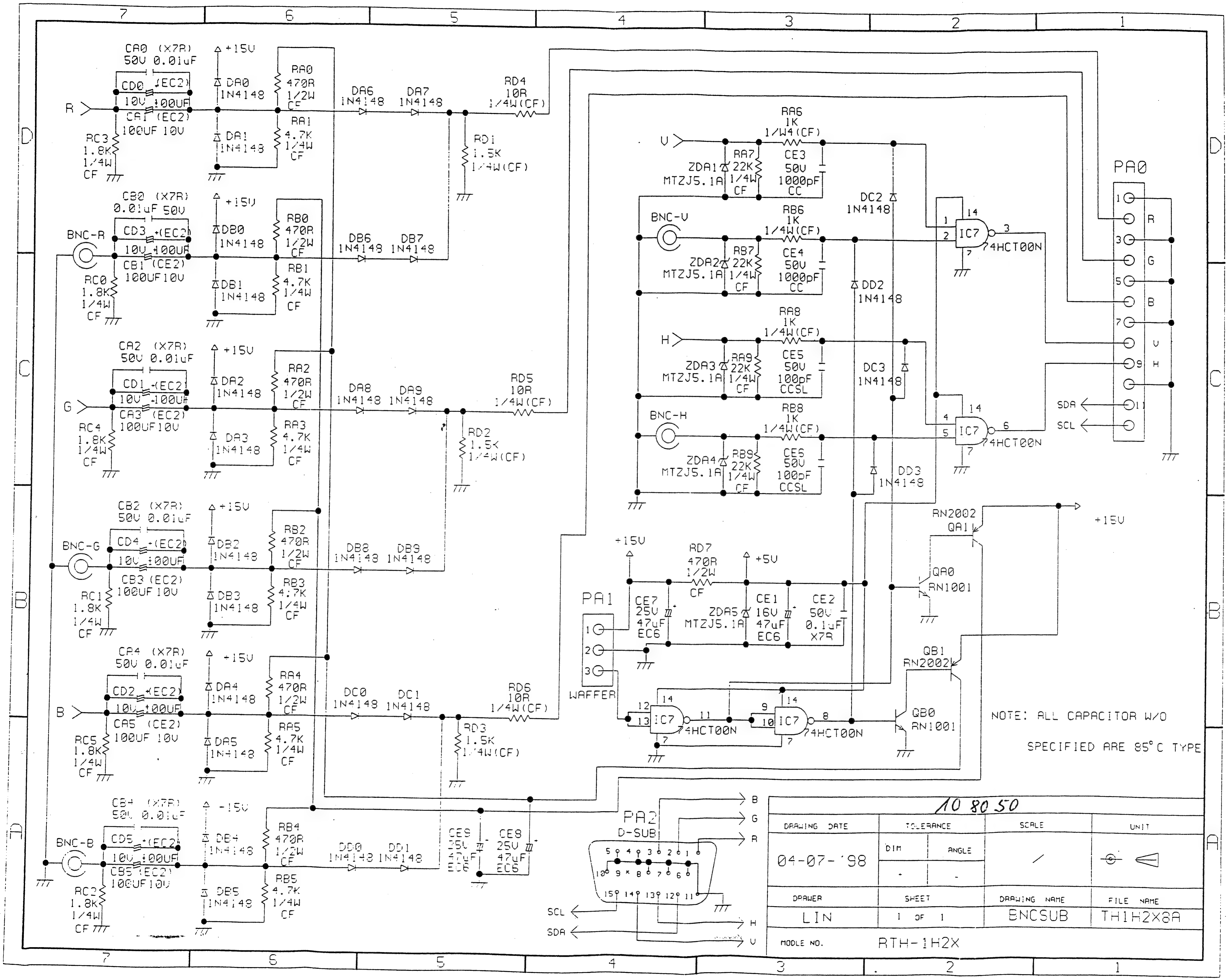
MODEL / LOCATION	BNC+DSUB TYPE 1H21/2/6	CAPTIVE TYPE 1H28/9
FT1	1R	22R
FT2	1R	68R
FT3	1R	68R
C4	12P	15P
C34	22P	39P
C54	22P	30P
FT4	2UH	0R
FT5	2UH	0R
FT6	2UH	0R
L1	22R 1/2W CC	0.39UH
L31	22R 1/2W CC	0.33UH
L51	22R 1/2W CC	0.39UH
R14	0.47UH	22R 1/2W CC
R44	0.47UH	22R 1/2W CC
R64	0.47UH	22R 1/2W CC

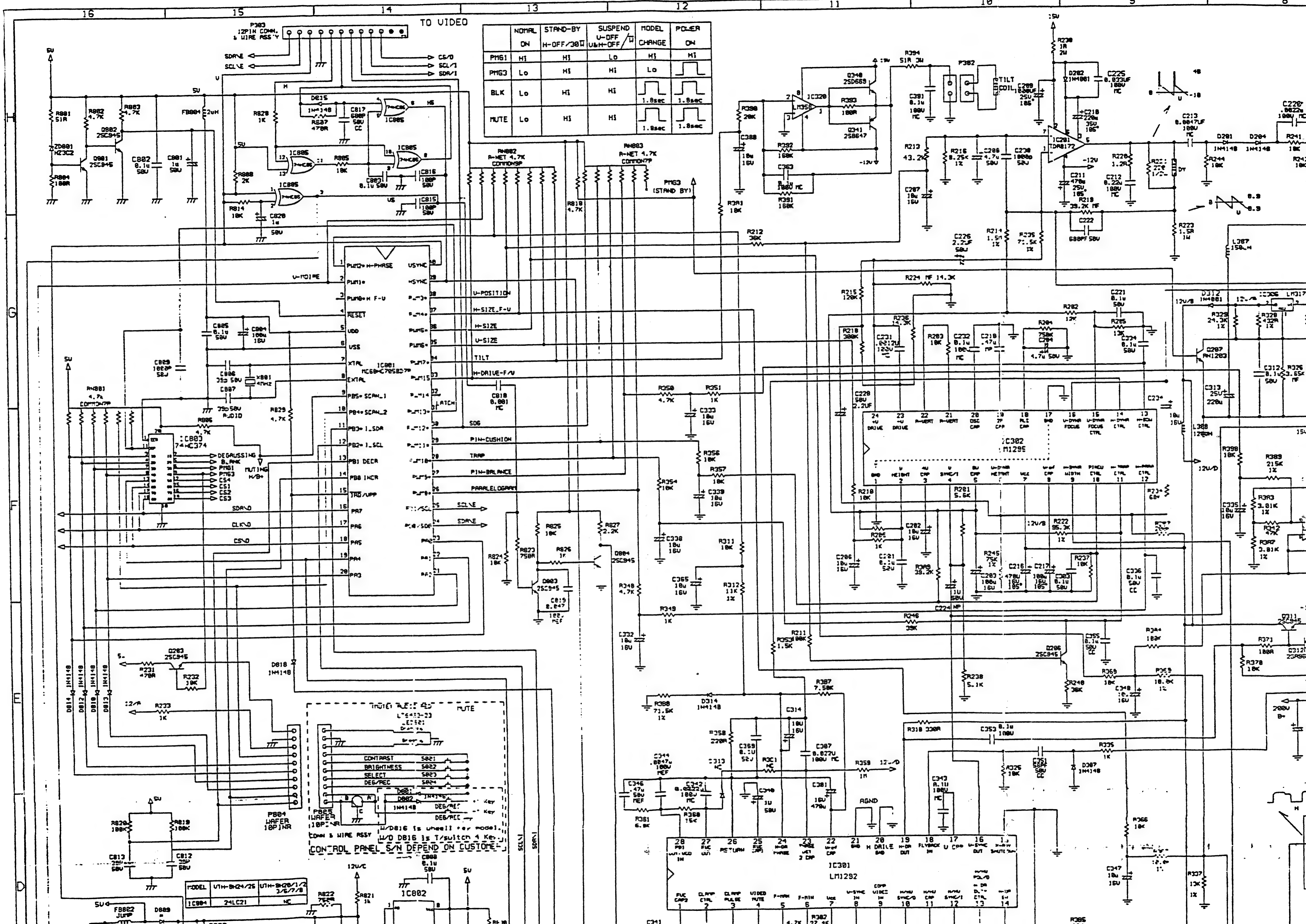
NOTE: ALL CAPACITOR W/O SPECIFIED VALUE ARE 85°C TYPE

10 80 50

DRAWING DATE	TOLERANCE		SCALE	UNIT
	DIM	ANGLE		
04-07-'98	- -	- -	/	mm
DRAWER	SHEET		DRAWING NAME	FILENAME
LIN	1 OF 1		NECK	TH1H2X2A

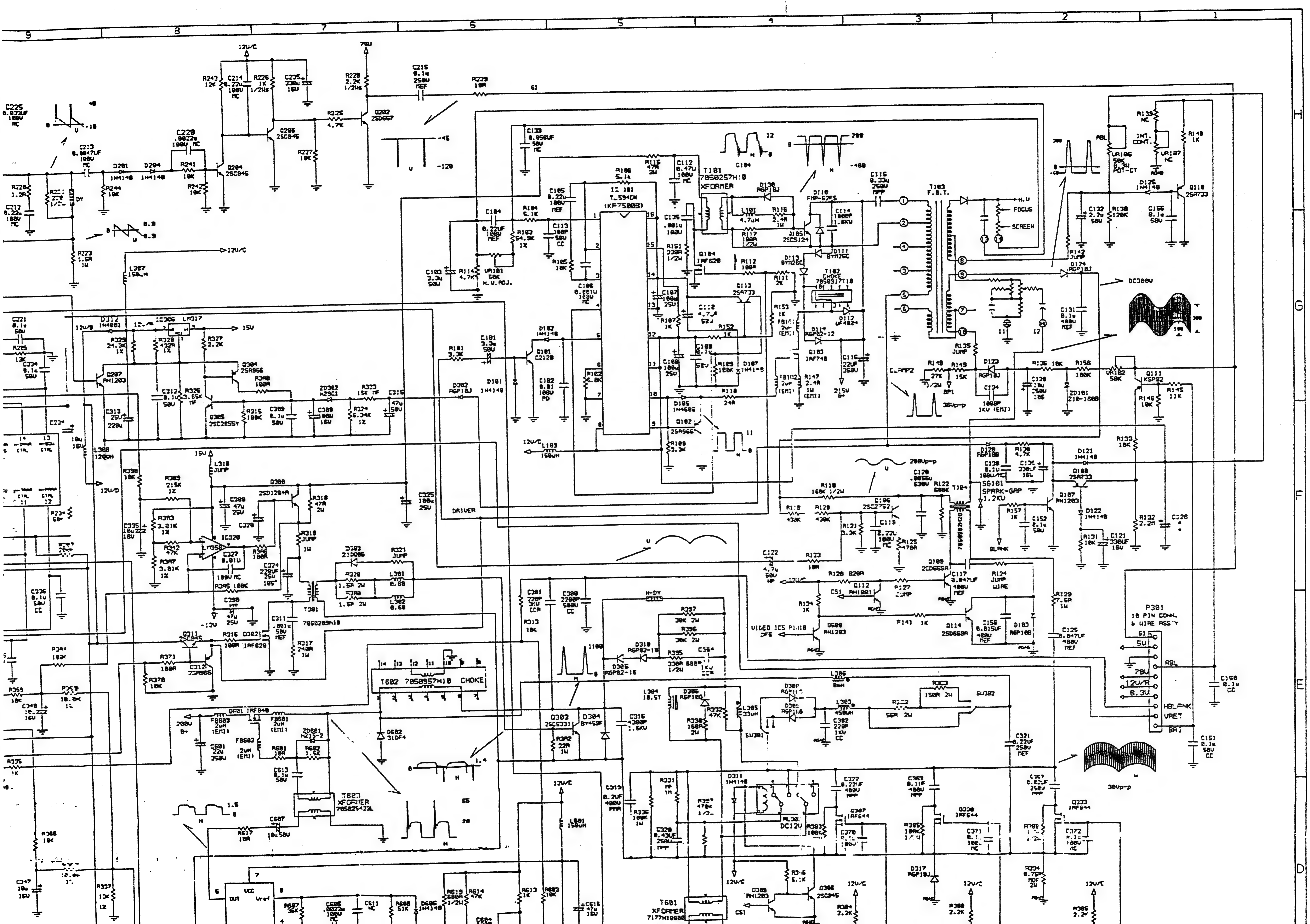
MODEL NO: RTH-1H2X


CA0 (X7R) 50V 0.01uF
CD0 (EC2) 10V 100UF
CA1 (EC2) 100UF 10V
RC3 1.8K 1/4W CF
R
+15V
DA0 1N4148
DA1 1N4148
RA0 470R 1/2W CF
RA1 4.7K 1/4W CF
DA6 1N4148
DA7 1N4148
RD4 10R 1/4W(CF)
RD1 1.5K 1/4W(CF)
CB0 (X7R) 0.01uF 50V
CD3 (EC2) 10V 100UF
CB1 (CE2) 100UF10V
BNC-R
RC0 1.8K 1/4W CF
DB0 1N4148
DB1 1N4148
RB0 470R 1/2W CF
RB1 4.7K 1/4W CF
DB6 1N4148
DB7 1N4148
CA2 (X7R) 50V 0.01uF
CD1 (EC2) 10V 100UF
CA3 (EC2) 100UF10V
G
RC4 1.8K 1/4W CF
DA2 1N4148
DA3 1N4148
RA2 470R 1/2W CF
RA3 4.7K 1/4W CF
DA8 1N4148
DA9 1N4148
RD5 10R 1/4W(CF)
RD2 1.5K 1/4W(CF)
CB2 (X7R) 50V 0.01uF
CD4 (EC2) 10V 100UF
CB3 (EC2) 100UF 10V
BNC-G
RC1 1.8K 1/4W CF
DB2 1N4148
DB3 1N4148
RB2 470R 1/2W CF
RB3 4.7K 1/4W CF
DB8 1N4148
DB9 1N4148
CA4 (X7R) 50V 0.01uF
CD2 (EC2) 10V 100UF
CA5 (CE2) 100UF 10V
B
RC5 1.8K 1/4W CF
DA4 1N4148
DA5 1N4148
RA4 470R 1/2W CF
RA5 4.7K 1/4W CF
DC0 1N4148
DC1 1N4148
RD6 10R 1/4W(CF)
RD3 1.5K 1/4W(CF)
CB4 (X7R) 50V 0.01uF
CD5 (EC2) 10V 100UF
CB5 (EC2) 100UF10V
BNC-B
RC2 1.8K 1/4W CF
DB4 1N4148
DB5 1N4148
RB4 470R 1/2W CF
RB5 4.7K 1/4W CF
DD0 1N4148
DD1 1N4148
CE9 25V 47uF EC6
CE8 25V 47uF EC6
V
RA6 1K 1/W4(CF)
RA7 22K 1/4W CF
ZDA1 MTZJ5.1A
CE3 50V 1000pF CC
BNC-V
RB6 1K 1/4W(CF)
RB7 22K 1/4W CF
ZDA2 MTZJ5.1A
CE4 50V 1000pF CC
H
RA8 1K 1/4W(CF)
RA9 22K 1/4W CF
ZDA3 MTZJ5.1A
CE5 50V 100pF CCSL
BNC-H
RB8 1K 1/4W(CF)
RB9 22K 1/4W CF
ZDA4 MTZJ5.1A
CE6 50V 100pF CCSL
DC2 1N4148
DD2 1N4148
DC3 1N4148
DD3 1N4148
IC7 74HCT00N
PA0
R
G
B
V
H
SDA
SCL
RN2002 QA1
QA0 RN1001
+15V
+5V
RD7 470R 1/2W CF
CE7 25V 47uF EC6
ZDA5 MTZJ5.1A
CE1 16V 47uF EC6
CE2 50V 0.1uF X7R
PA1
WAFFER
QB1 RN2002
QB0 RN1001
PA2 D-SUB
NOTE: ALL CAPACITOR W/O SPECIFIED ARE 85°C TYPE
10 80 50
DRAWING DATE 04-07-'98
TOLERANCE DIM ANGLE
SCALE
UNIT
DRAWER LIN
SHEET 1 OF 1
DRAWING NAME BNCSUB
FILE NAME TH1H2X8A
MODLE NO. RTH-1H2X

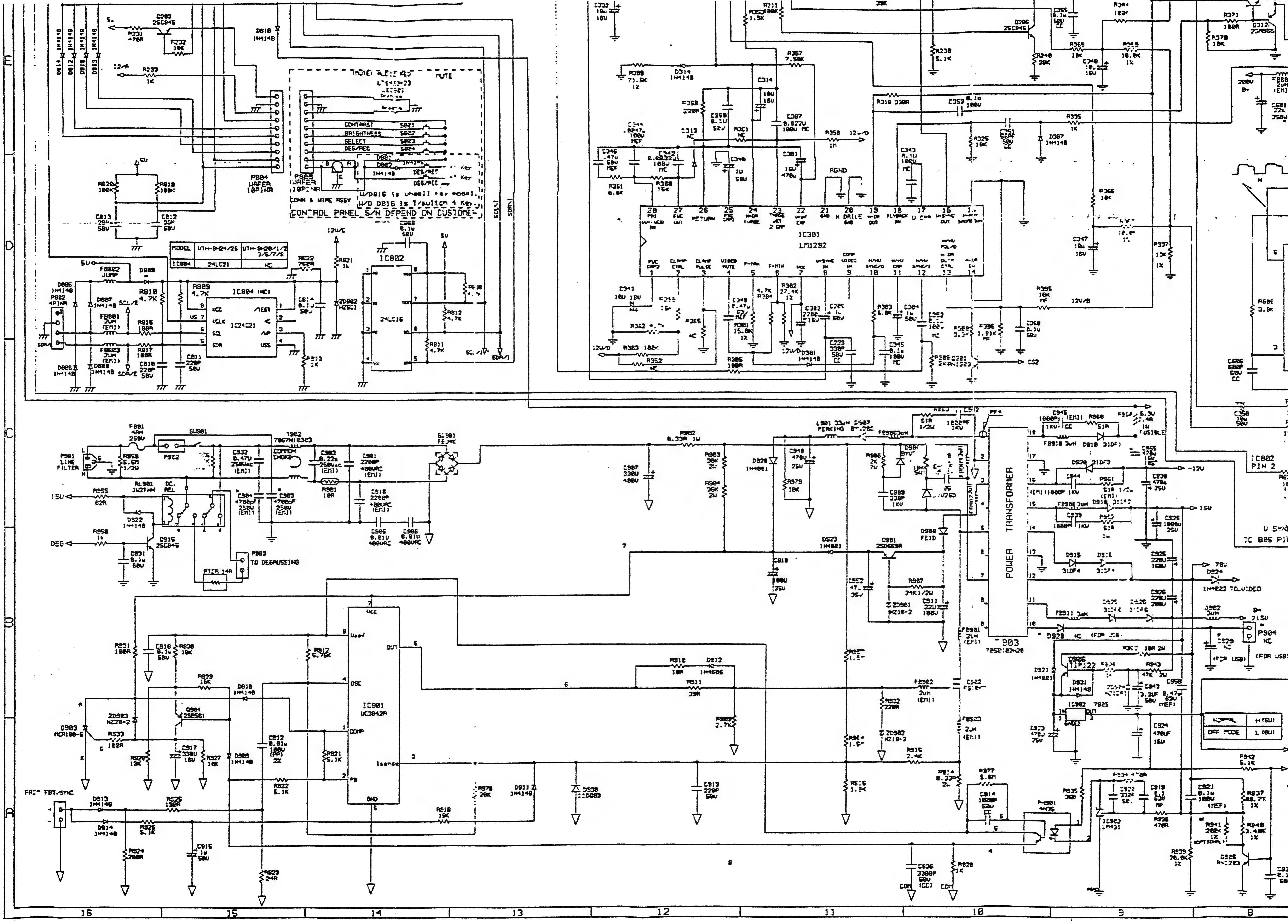


	NOMAL ON	STAND-BY H-OFF/30	SUSPEND V-OFF V&H-OFF	MODEL CHANGE	POWER ON
PMG1	Hi	Hi	Lo	Hi	Hi
PMG3	Lo	Hi	Hi	Lo	
BLK	Lo	Hi	Hi	1.8sec	1.8sec
MUTE	Lo	Hi	Hi	1.8sec	1.8sec

MODEL	UTH-BH24/26	UTH-BH20/1/2 3/6/7/8
IC804	24LC21	NC



9
8
7
6
5
4
3
2
1
H
G
F
E
D
12V/C
78V
IC 101
T_594CM
(KF7500B)
T101
7050257H10
XFORMER
T103
F.B.T.
H.V
FOCUS
SCREEN
T102
CHOKE
7050917T10
DC300V
CLAMP2
36Vp-p
200Vp-p
SG101
SPARK-GAP
1.2KV
BLANK
DRIVER
P301
10 PIN CONN.
& WIRE ASS'Y
5V
78V
12V/R
6.3V
ABL
HBLANK
VRET
BRI
T602 7050957H10 CHOKE
T620
XFORMER
7050251423L
T601
XFORMER
7177H10000
T301
7050289H10
VIDEO ICS P1.10
SW301
SW302
RL301
DC12V
H.V.ADJ.
ABL
INT.
CONT.
POT-CT
H-DY
30Vp-p
200V
B+
215V
B+
15V
-12V
LM317
LM358



CONTRAST
BRIGHTNESS
SELECT
DEG/REC
W/D816 is used for model
W/O D816 is T/switch 4 Key
CONTROL PANEL S/W DEPEND ON CUSTOMER
P804
WAFER
10PIN R
MODEL
24LC21
IC804
IC802
24LC16
IC301
LM1292
AGND
LINE FILTER
COMMON CHOKE
TO DEGAUSSING
IC901
UC3842A
POWER TRANSFORMER
FROM FBT/SYNC
TO VIDEO
V SYNC
OFF MODE
16
15
14
13
12
11
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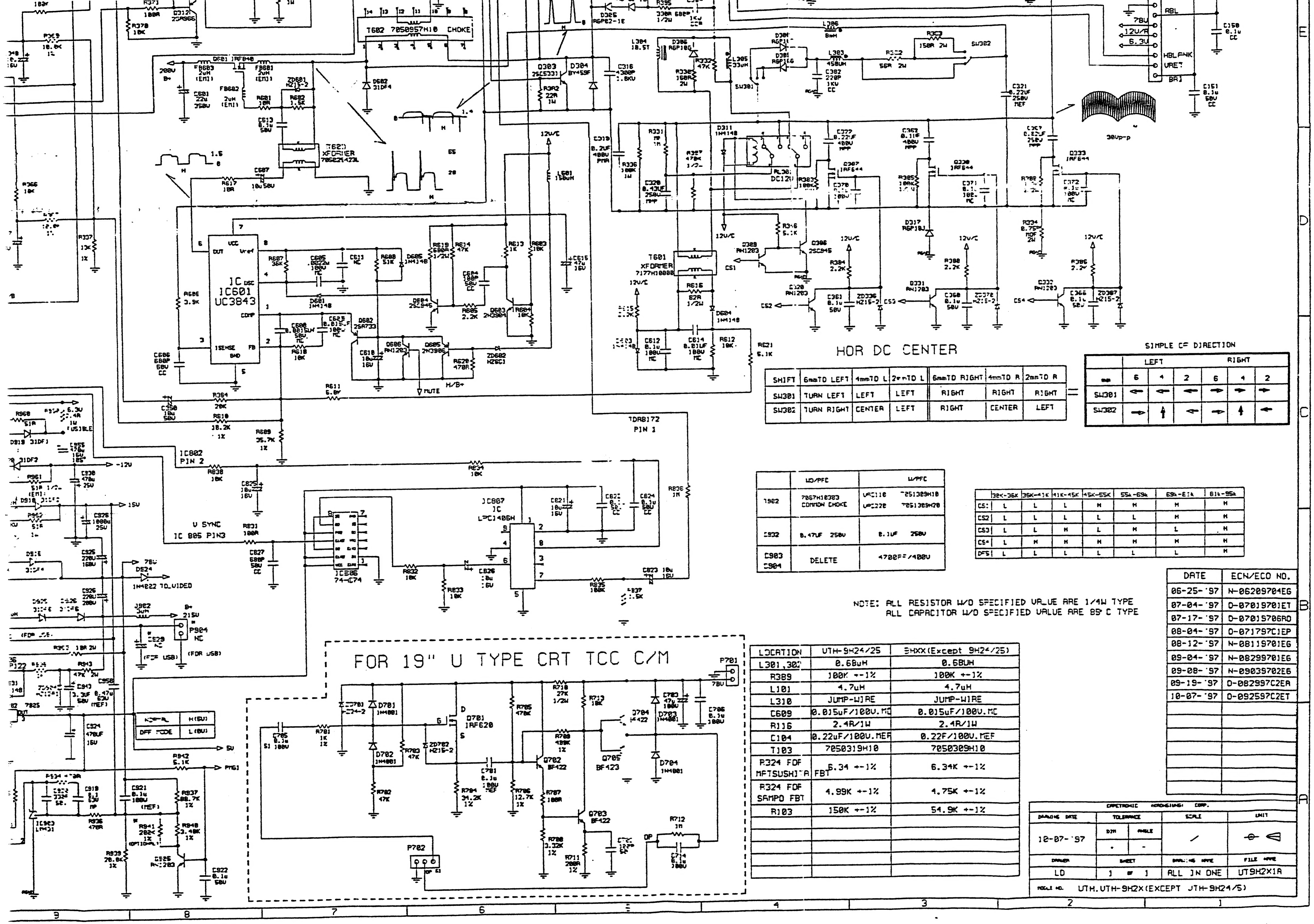
9
8



HOR DC CENTER

SHIFT	6mmTO LEFT	4mmTO L	2mmTO L	6mmTO RIGHT	4mmTO R	2mmTO R
SW301	TURN LEFT	LEFT	LEFT	RIGHT	RIGHT	RIGHT
SW302	TURN RIGHT	CENTER	LEFT	RIGHT	CENTER	LEFT

SIMPLE CF DIRECTION

	LEFT			RIGHT		
mm	6	4	2	6	4	2
SW301	←	←	←	→	→	→
SW302	→	↑	←	→	↑	←

	WO/PFC	W/PFC
T902	7067H10303 COMMON CHOKE	VAC110 7251309H10 VAC220 7251309H20
C932	0.47UF 250V	0.1UF 250V
C903 C904	DELETE	4700PF/400V

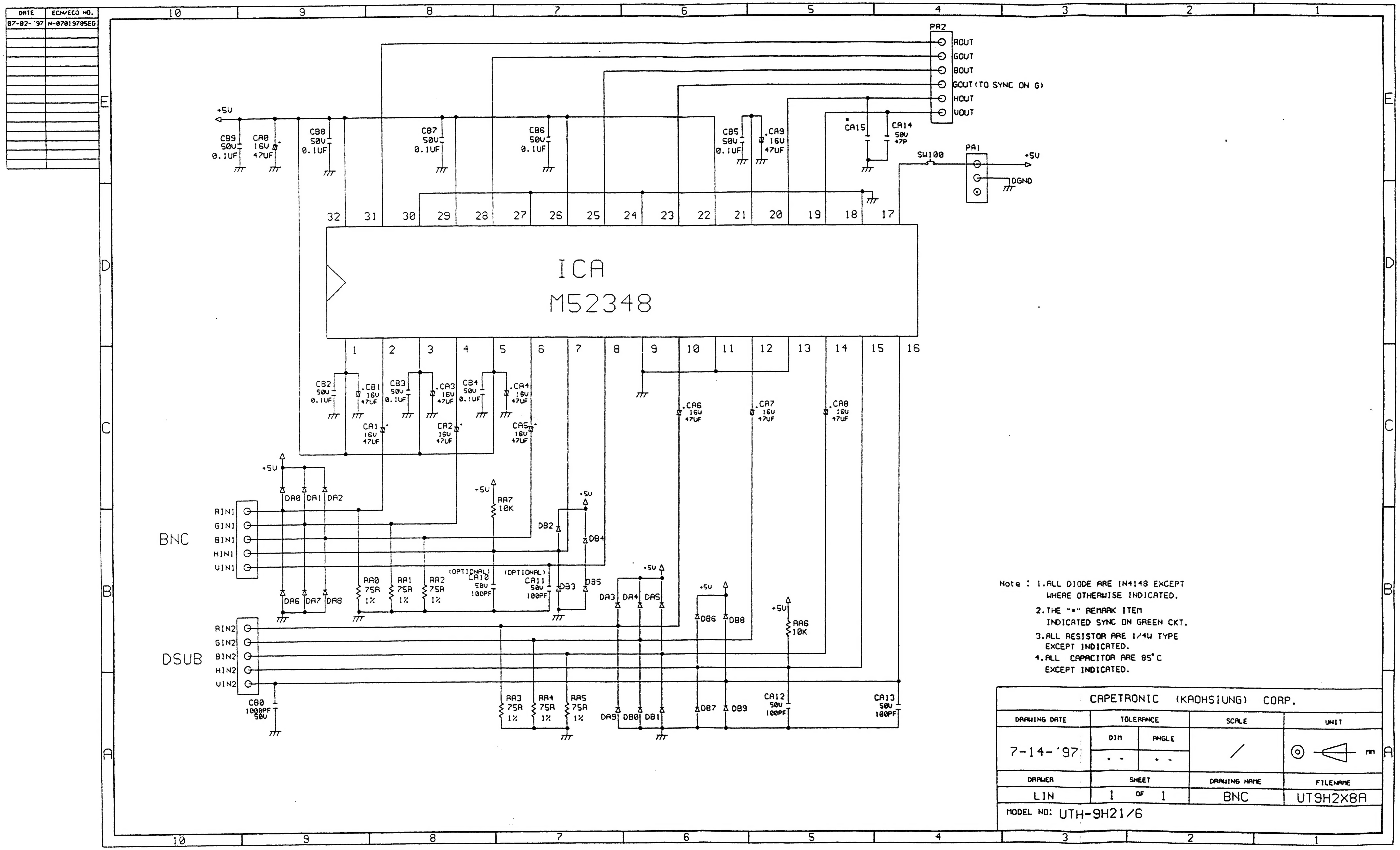
	30K-36K	35K-41K	41K-45K	45K-55K	55k-69k	69k-81k	81k-95k
CS1	L	L	L	H	H	H	H
CS2	L	L	L	L	L	H	H
CS3	L	L	H	L	H	L	H
CS4	L	H	H	H	H	H	H
DFS	L	L	L	L	L	L	H

NOTE: ALL RESISTOR W/O SPECIFIED VALUE ARE 1/4W TYPE
ALL CAPACITOR W/O SPECIFIED VALUE ARE 85°C TYPE

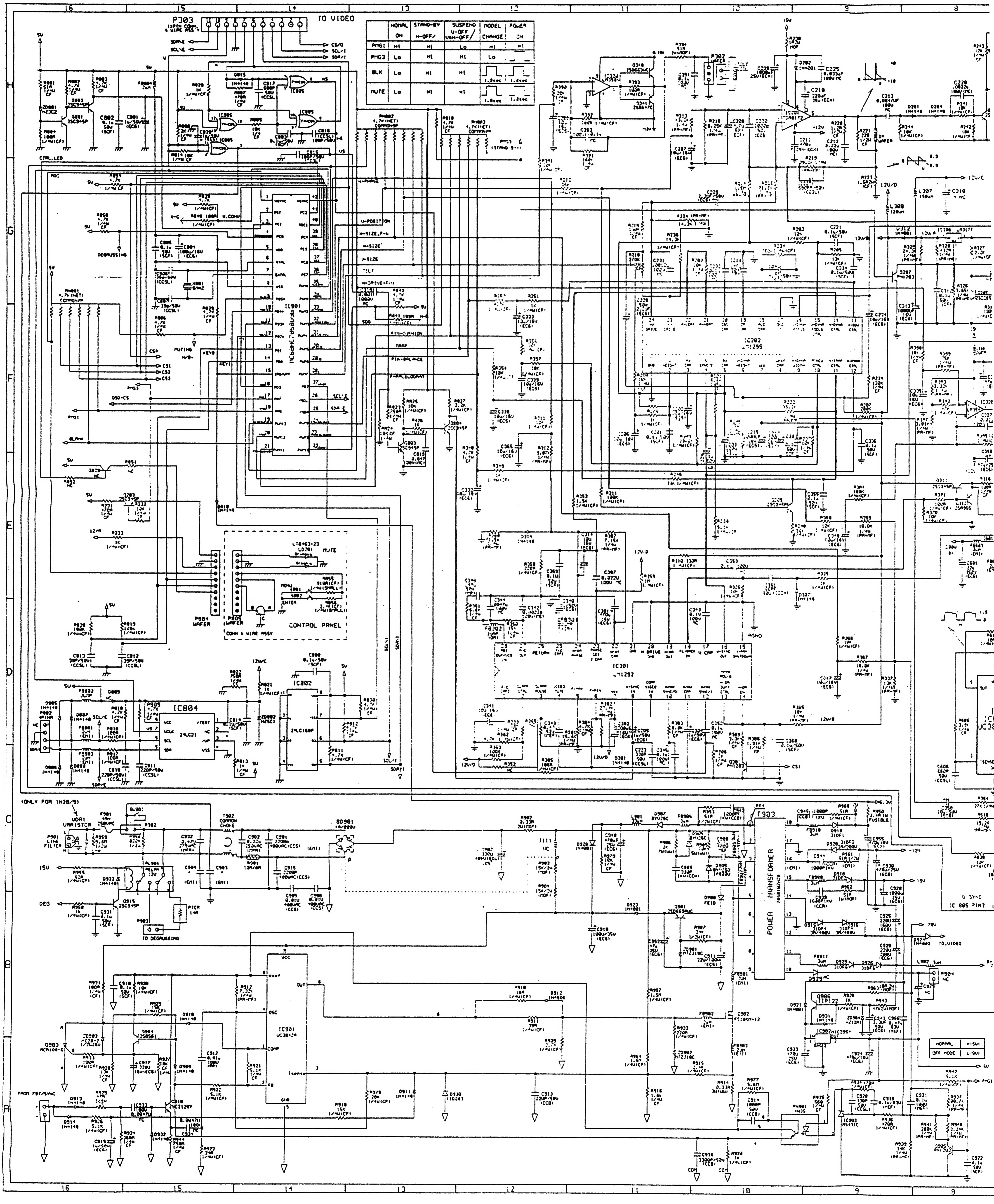
LOCATION	UTH-9H24/25	9HXX(Except 9H24/25)
L301,302	0.68uH	0.68UH
R389	100K +-1%	100K +-1%
L101	4.7uH	4.7uH
L310	JUMP-WIRE	JUMP-WIRE
C609	0.015uF/100V.MC	0.015uF/100V.MC
R116	2.4R/1W	2.4R/1W
C104	0.22uF/100V.MEF	0.22F/100V.MEF
T103	7050319H10	7050309H10
R324 FOF MATSUSHITA FBT	6.34 +-1%	6.34K +-1%
R324 FOF SAMPO FBT	4.99K +-1%	4.75K +-1%
R103	150K +-1%	54.9K +-1%

DATE	ECN/ECO NO.
06-25-'97	N-06209704EG
07-04-'97	O-07019701ET
07-17-'97	O-07015706RO
08-04-'97	O-071797C1EP
08-12-'97	N-08119701EG
09-04-'97	N-08299701E6
09-08-'97	N-09039702E6
09-19-'97	O-082997C2EA
10-07-'97	O-092597C2ET

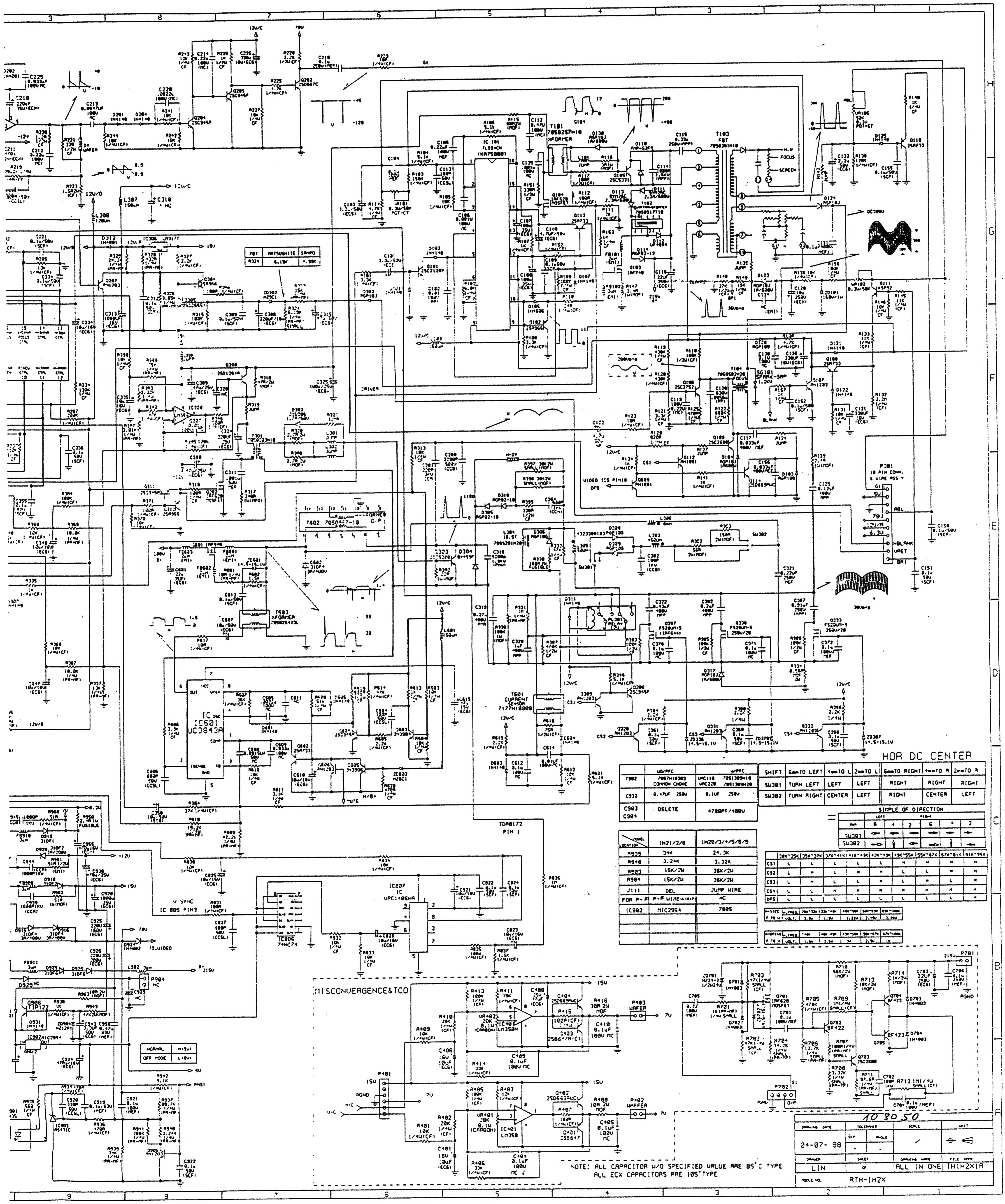
CAPETRONIC (KOROHSIUNG) CORP.				
DRAWING DATE	TOLERANCE		SCALE	UNIT
10-07-'97	DIM	ANGLE	/	
	.	-		
DRAWER	SHEET		DRAWING NAME	FILE NAME
LD	1 OF 1		ALL IN ONE	UT9H2X1A
MODEL NO.	UTH.UTH-9H2X(EXCEPT UTH-9H24/5)			



VIDE-V20481 / DRUCK2



P303
TO VIDEO
IC801
IC804
24LC21
IC802
24LC16BP
CONTROL PANEL
COMM & WIRE ASSY
IC302
IC301
POWER TRANSFORMER
T903
IC901
(ONLY FOR 1H28/91)
LINE FILTER
TO DEGAUSSING
DEGAUSSING
FROM FBT/SYNC



	W/O PFC	W/PFC
T902	7067H10303 COMMON CHOKE	VAC110 7051309H10 VAC220 7051309H20
C932	0.47UF 250V	0.1UF 250V
C903 C904	DELETE	4700PF/400V

SHIFT	6mm TO LEFT	4mm TO L	2mm TO L	6mm TO RIGHT	4mm TO R	2mm TO R
SW301	TURN LEFT	LEFT	LEFT	RIGHT	RIGHT	RIGHT
SW302	TURN RIGHT	CENTER	LEFT	RIGHT	CENTER	LEFT

LOCATION \ MODEL	1H21/2/6	1H20/3/4/5/8/9
R939	34K	24.3K
R940	3.24K	3.32K
R903	15K/2W	36K/2W
R904	15K/2W	36K/2W
J111	DEL	JUMP WIRE
FOR P-P	P-P WIRE	NC
IC902	MIC2954	7805

	30K~35K	35K~37K	37K~41K	41K~43K	43K~49K	49K~55K	55K~67K	67K~81K	81K~95K
CS1	L	L	L	L	L	H	H	H	H
CS2	L	H	L	H	H	L	L	H	H
CS3	L	H	L	H	L	H	L	H	H
CS4	L	L	H	H	H	H	H	H	H
DFS	L	L	L	L	L	L	L	L	H

NOTE: ALL CAPACITOR W/O SPECIFIED VALUE ARE 85°C TYPE
ALL ECX CAPACITORS ARE 105° TYPE

10 80 50

DRAWING DATE	TOLERANCE	SCALE	UNIT
04-07-'98		/	
DRAWER	SHEET	DRAWING NAME	FILE NAME
LIN	OF	ALL IN ONE	TH1H2X1A
MODLE NO.	RTH-1H2X		